

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR LETTERS PATENT

Title : SEMICONDUCTOR DEVICE AND METHOD OF
FABRICATING THE SAME

Inventor(s) : Shigeo SATOH
Masataka KASE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2002-254672, filed on August 30, 2002, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[Field of the Invention]

This invention relates to a semiconductor device having a gate and source-and-drain regions, and a method of fabricating thereof, which are particularly preferable when applied to a CMOS transistor.

[Description of the Related Art]

Conventional CMOS transistors generally employ a polysilicon gate electrode doped with an n-type impurity for the n-channel MOS transistor (nMOS transistor) composing thereof. This is because the threshold voltage can readily be controlled to desired values. The nMOS transistor is turned ON when applied with a positive voltage through the gate electrode, which causes bending of the energy band of polysilicon, and generates a depletion layer within the gate electrode in the vicinity of the interface with a gate insulating film. Such production of the depletion layer undesirably lowers the gate capacitance and thus reduces ON current. To suppress

the lowering of the gate capacitance, it is necessary to raise concentration of the n-type impurity within the gate electrode in the vicinity of the interface with the gate insulating film.

The same will apply to the p-channel MOS transistor (pMOS transistor) which employs a polysilicon gate electrode doped with a p-type impurity, where it is also necessary to raise concentration of the p-type impurity within the gate electrode in the vicinity of the interface with the gate insulating film in order to suppress lowering of the gate capacitance during the ON status.

In a general procedure for fabricating the aforementioned nMOS and pMOS transistors, the source-and-drain regions are formed by ion implantation, where the gate electrodes which serve as masks are also concomitantly doped.

To suppress lowering in the gate capacitance, it is necessary to suppress formation of the depletion layer within the gate electrode, and it is thus necessary to raise the dose of the impurity introduced into the gate electrode, which impurity is concomitantly doped also into the source-and-drain regions. This successfully raises the impurity concentration within the gate electrode, but also raises the impurity concentration in the source-and-drain regions, which undesirably promotes lateral diffusion of the impurity in the source-and-drain

regions, and results in degradation of short-channel resistance.

One known solution for addressing the problem relates to reduction in height of the gate electrode, which can substantially increase the impurity concentration even if the dose of impurity introduced to the gate electrode remains unchanged. This solution, however, raises another problem that too low height of the gate electrode may result in punch-through of the impurity introduced into the gate electrode into the channel, which undesirably varies the threshold voltage. The technique for reducing the height of gate electrode is thus limitative.

SUMMARY OF THE INVENTION

The present invention is thus to provide a highly-reliable semiconductor device and a method of fabricating thereof, both of which are aimed at raising impurity concentration within the gate electrode without increasing impurity concentration in the source-and-drain regions, and as a consequence at improving gate capacitance and short-channel resistance without anticipating fluctuation in the threshold voltage due to variation in shape of the gate electrode.

After extensive investigations and discussions, the present inventors reached the various aspects of the present invention described below.

A method of fabricating a semiconductor device according to one aspect of the present invention comprises a first step of patterning a gate electrode above a semiconductor substrate having an element isolation structure previously formed therein; a second step of forming sidewalls covering only on both side faces of the gate electrode; a third step of removing the upper portion of the sidewalls to thereby expose a part of both side faces of the gate electrode; and a fourth step for introducing an impurity into the gate electrode along a direction inclined to the surface of the semiconductor substrate.

A method of fabricating a semiconductor device according to another aspect of the present invention comprises a first step of patterning a gate electrode above a semiconductor substrate; a second step of forming a mask having an opening which allows the gate electrode to be exposed therein; and a third step of introducing an impurity into the gate electrode along a direction inclined to the surface of the semiconductor substrate, wherein in the second step, the opening of the mask is formed in a size which ensures protection of areas for forming source-and-drain regions on both sides of the gate electrode from the tilt-angle introduction of the impurity.

A semiconductor device according to one aspect of the present invention comprises a gate electrode;

source-and-drain regions; sidewalls covering only the lower portion of both side faces of the gate electrode; and a silicide film formed on the exposed surface of the gate electrode, wherein the gate electrode contains an impurity having a conductivity type same as that of the impurity contained in the source-and-drain regions, and the gate electrode has an impurity concentration larger than that of the source-and-drain regions.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic sectional view showing a major principle of a first technique;

Fig. 2 is a schematic sectional view showing a major principle of a second technique;

Fig. 3 is a schematic sectional view showing an exemplary case of a combination of the first and second techniques;

Figs. 4A to 4D are schematic sectional views sequentially showing process steps of a method of fabricating a CMOS transistor according to a first embodiment;

Figs. 5A to 5D are schematic sectional views sequentially showing process steps as continued from Fig. 4D;

Figs. 6A and 6B are schematic sectional views sequentially showing process steps as continued from Fig. 5D;

Figs. 7A to 7D are schematic sectional views sequentially showing process steps as continued from Fig. 6B;

Figs. 8A to 8D are schematic sectional views sequentially showing process steps as continued from Fig. 7D;

Fig. 9 is a plan view for explaining tilt-angled ion implantation;

Fig. 10 is a plan view for explaining a modified example of tilt-angled ion implantation in the first embodiment;

Figs. 11A to 11D are schematic sectional views sequentially showing major process steps of a method of fabricating a CMOS transistor according to a second embodiment;

Figs. 12A to 12D are sequentially showing major process steps of a method of fabricating a CMOS transistor according to a third embodiment;

Figs. 13A to 13D are schematic sectional views sequentially showing process steps as continued from Fig. 12D;

Fig. 14 is a plan view for explaining tilt-angled ion implantation;

Figs. 15A to 15D are schematic sectional views sequentially showing major process steps of a method of fabricating a CMOS transistor according to a fourth embodiment;

Figs. 16A to 16D are schematic sectional views sequentially showing process steps as continued from Fig. 15D;

Fig. 17 is a plan view for explaining tilt-angled ion implantation;

Figs. 18A to 18D are schematic sectional views sequentially showing major process steps of a method of fabricating a CMOS transistor according to a fifth embodiment;

Figs. 19A to 19D are schematic sectional views sequentially showing process steps as continued from Fig. 18D;

Fig. 20 is a plan view for explaining tilt-angled ion implantation;

Figs. 21A to 21D are schematic sectional views sequentially showing major process steps of a method of fabricating a CMOS transistor according to a sixth embodiment;

Figs. 22A to 22D are schematic sectional views sequentially showing process steps as continued from Fig. 21D;

Figs. 23A to 23D are schematic sectional views sequentially showing process steps as continued from Fig. 22D;

Fig. 24 is a plan view for explaining tilt-angled ion implantation;

Figs. 25A to 25D are schematic sectional views sequentially showing major process steps of a method

of fabricating a CMOS transistor according to a seventh embodiment;

Figs. 26A to 26D are schematic sectional views sequentially showing process steps as continued from Fig. 25D;

Figs. 27A to 27C are schematic sectional views sequentially showing process steps as continued from Fig. 26D;

Figs. 28A to 28C are schematic sectional views sequentially showing process steps of a method of fabricating a CMOS transistor according to a modified example of the seventh embodiment;

Figs. 29A to 29C are schematic sectional views sequentially showing process steps as continued from Fig. 28C;

Figs. 30A to 30D are schematic sectional views sequentially showing major process steps of a method of fabricating a CMOS transistor according to a eighth embodiment;

Figs. 31A to 31D are schematic sectional views sequentially showing process steps as continued from Fig. 30D;

Figs. 32A to 32D are schematic sectional views sequentially showing process steps as continued from Fig. 31D;

Figs. 33A to 33D are schematic sectional views sequentially showing major process steps of a method

of fabricating a CMOS transistor according to a ninth embodiment;

Figs. 34A to 34C are schematic sectional views sequentially showing process steps as continued from Fig. 33D;

Fig. 35 is a schematic drawing for explaining a method of determining an alignment rule of a resist mask with respect to the gate electrode in the fourth and fifth embodiments;

Fig. 36 is a schematic drawing for explaining a method of determining an alignment rule of a resist mask with respect to the aligned gate electrodes in the fourth and fifth embodiments;

Fig. 37 is a characteristic chart showing a method of determining an alignment rule of a resist mask with respect to the aligned gate electrodes in the fourth and fifth embodiments;

Fig. 38 is a schematic drawing for explaining a method of determining an alignment rule of a resist mask with respect to the gate electrode in the sixth through ninth embodiments;

Fig. 39 is a schematic drawing for explaining a method of determining an alignment rule of a resist mask with respect to the aligned gate electrodes in the sixth through ninth embodiments;

Fig. 40 is a characteristic chart showing a method of determining an alignment rule of a resist

mask with respect to the aligned gate electrodes in the sixth through ninth embodiments; and

Fig. 41 is a block diagram showing an internal constitution of a general personal user terminal device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

- Basic Concept of the Present Invention -

First a basic concept of a major constitution of the present invention will be described.

In pursuit of solving the aforementioned problems, the present inventors reached an idea of a semiconductor device in which the gate electrode is designed to have an impurity concentration higher than that of the source-and-drain regions, and proposed, as a specific technique for realizing such semiconductor device, a method of fabricating thereof as explained below.

(First Technique)

A major principle of a first technique is shown in Fig. 1.

First, sidewalls 103 are formed on both side faces of a gate electrode 102. Portions of a semiconductor substrate 101 which fall on both sides of the gate electrode 102 and sidewalls 103 serve as source-and-drain (S/D) regions 104, respectively.

Next, the sidewalls 103 are over-etched to thereby allow the upper portion of the gate electrode

102 to be exposed. The gate electrode 102 herein is remained so as to expose an area extending from the top surface thereof to the upper portion of both side faces thereof.

Next, an impurity having a conductivity same as that doped in the source-and-drain regions is then implanted into the exposed surface of the gate electrode 102 from a direction inclined to the surface of the semiconductor substrate 101.

The gate electrode 102 herein is doped with the impurity in its top surface and in the upper portion of one side face (indicated with reference numeral 102a in the figure). Since the impurity can rapidly diffuse in polysilicon, the impurity rapidly diffuses during the later annealing to thereby attain a uniform distribution. That is, carrying out of the tilt-angled ion implantation is nearly worth ion implantation repeated twice, and can raise the impurity concentration at the interface with the gate insulating film as compared with that attainable by vertical ion implantation.

On the contrary, either of the source-and-drain regions 104 is introduced with the impurity only in a dose corresponding to a single implantation (indicated with reference numeral 104a in the figure), where the other region is not introduced at all, or only slightly introduced (indicated with reference numeral 104b) although being almost not influential.

Therefore by repeating the tilt-angled ion implantation in a plural number of times, the impurity concentration of the gate electrode 102 can be raised to a desired degree as compared with that of the source-and-drain regions 104, while varying the direction of implantation [typically once each in the directions opposed along the width of the gate electrode 102 (referred to as a direction normal to the gate length, hereinafter) and once each in the directions opposed along the length of the gate electrode (referred to as a direction parallel to the gate length)].

(Second Technique)

A major principle of a second technique is shown in Fig. 2.

In this technique, a resist mask 105 having an opening 105a, which is formed in a size allowing the gate electrode 102 to expose therein and allowing the source-and-drain regions 104 to be protected (prevented) from the tilt-angled ion implantation, is formed, and the tilt-angled ion implantation is carried out in this situation. Also in this case, the tilt-angled ion implantation is carried out in a plural number of times while varying the direction of implantation.

The gate electrode 102 herein is doped with the impurity in its top surface and in the upper portion of one side face (indicated with reference numeral

102a in the figure). Since the impurity can rapidly diffuse in polysilicon, the impurity rapidly diffuses during the later annealing to thereby attain a uniform distribution. That is, a single tilt-angled ion implantation is nearly worth ion implantation repeated twice, and can raise the impurity concentration at the interface with the gate insulating film as compared with that attainable by vertical ion implantation.

On the contrary, a pair of source-and-drain regions 104 protected by the resist mask 105 are prevented from being introduced with the impurity.

Since increase in the impurity concentration in the gate electrode 102 does not affect or increase the impurity concentration of the source-and-drain regions 104 as described in the above, short-channel effect is certainly prevented from being worsened.

It is to be noted now that it is also allowable, as shown in Fig. 3, to over-etch the sidewalls 103 so as to expose the upper portion of both side faces of the gate electrode 102 as described in the first technique, and then to form the resist mask 105 having the opening 105a formed in a size which ensures protection (prevention) of the source-and-drain regions 104 from the tilt-angled ion implantation as described in the second technique, and to carry out the tilt-angled ion implantation in this situation. This ensures introduction of the

impurity only into the gate electrode 102 in a more precise manner.

- Specific Embodiments -

Based on the basic concept of the present invention described in the above, specific embodiments whereby the present invention is applied to a CMOS transistor will be explained with reference to the attached drawings.

(First Embodiment)

Figs. 4A through 8D are schematic sectional views sequentially showing process steps of a method of fabricating a CMOS transistor.

First as shown in Fig. 4A, trenches are formed in an element isolation region of a semiconductor substrate 1, filled with an insulating material such as silicon oxide, and the surface thereof is planarized typically by CMP (chemical mechanical polishing) to thereby form a STI-type (shallow trench isolation-type) element isolation structures 2. This partitions element active regions on the semiconductor substrate 1, which are an nMOS region 11 and a pMOS region 12.

Next, as shown in Fig. 4B, a resist mask 13 is formed so as to cover the pMOS region 12, and a p-type impurity is introduced by ion implantation into the nMOS region 11, to thereby form a p-well 3, and a channel stopper layer (not shown) in the surficial portion of the substrate.

Next, the resist mask 13 is removed typically by ashing, a resist mask 14 is formed so as to cover the nMOS region 11 as shown in Fig. 4C, and an n-type impurity is introduced by ion implantation into the pMOS region 12, to thereby form an n-well 4, and a channel stopper layer (not shown) in the surficial portion of the substrate.

Next, the resist mask 14 is removed typically by ashing, and, as shown in Fig. 4D, the semiconductor substrate 1 is then annealed by RTA (rapid thermal annealing) at 1,000°C for 3 seconds to thereby restore the substrate from damage caused by introduction of the impurities into the wells 3, 4 and channel stopper layers.

Next, as shown in Fig. 5A, a thin gate insulating film 5 is formed on the surface of the semiconductor substrate 1 by thermal oxidation, and further thereon, a non-doped polysilicon film 15 is deposited by the CVD process as shown in Fig. 5B.

Next, the polysilicon film 15 and the gate insulating film 5 are patterned by photolithography and succeeding dry etching to thereby form gate electrodes 6a, 6b of approx. 100 nm high and approx. 50 nm wide on the gate insulating film 5 in the nMOS and pMOS regions 11, 12, respectively, as shown in Fig. 5C. In this process, the polysilicon film 15 has no impurity previously introduced therein, because polysilicon doped with an n-type impurity and that doped with a p-type impurity generally differ in

the etchrate, which makes it difficult to form respective gate electrodes of nMOS transistor and pMOS transistor at a same time.

Next, as shown in Fig. 5D, a resist mask 16 is formed so as to cover the pMOS region 12, and an n-type impurity, which is arsenic (As) herein, is introduced by vertical ion implanted into the nMOS region 11 at an ion acceleration energy of 5 keV and a dose of $6 \times 10^{14}/\text{cm}^2$, and also a p-type impurity, which is boron (B) herein, is introduced by ion implantation at an ion acceleration energy of 10 keV, a dose of $8 \times 10^{12}/\text{cm}^2$, and an angle of incidence of 30° from four directions, to thereby form n-type extension layers 7a and p-type pocket layers 8a, respectively.

Next, the resist mask 16 is removed typically by ashing, a resist mask 17 is formed so as to cover the nMOS region 11 as shown in Fig. 6A, and a p-type impurity, which is boron (B) herein, is introduced by vertical ion implantation into the pMOS region 12 at an ion acceleration energy of 0.5 keV and a dose of $6 \times 10^{14}/\text{cm}^2$, and also an n-type impurity, which is arsenic (As) herein, is introduced by ion implantation at an ion acceleration energy of 50 keV, a dose of $6 \times 10^{12}/\text{cm}^2$, and an angle of incidence of 30° from four directions, to thereby form p-type extension layers 7b and n-type pocket layers 8a, respectively.

Next, as shown in Fig. 6B, the resist mask 17 is removed typically by ashing, and, as shown in Fig. 6B, the semiconductor substrate 1 is then annealed by RTA (rapid thermal annealing) at 1,000°C for one second to thereby restore the substrate from damage generated by introduction of the impurities into the extension layers 7a, 7b and pocket layers 8a, 8b.

Next, a silicon oxide film (not shown) is deposited on the entire surface by the CVD process, and the film is then anisotropically etched back so as to allow the film to remain only on both side faces of the gate electrodes 6a, 6b, to thereby form sidewalls 9a, 9b having a maximum width of 80 nm or around, as shown in Fig. 7A.

Next, a resist mask 18 is formed so as to cover the pMOS region 12 as shown in Fig. 7B, and an n-type impurity, which is phosphorus (P) herein, is introduced by ion implantation into the nMOS region 11 at an ion acceleration energy of 8 keV, a dose of $4.5 \times 10^{15}/\text{cm}^2$, and an angle of incidence of 0° (that is, normal to the surface of the substrate), to thereby form the n-type, source-and-drain regions 10a. Phosphorus herein is also implanted into the gate electrode 6a. The dose of phosphorus in this process is controlled to a smaller value ($6 \times 10^{15}/\text{cm}^2$, for example) than that in general formation process of n-type, source-and-drain regions.

Next, the resist mask 18 is removed typically by ashing, a resist mask 19 is formed so as to cover the nMOS region 11 as shown in Fig. 7C, and a p-type impurity, which is boron (B) herein, is introduced by ion implantation into the pMOS region 12 at an ion acceleration energy of 4 keV, a dose of $2.25 \times 10^{15}/\text{cm}^2$ and an angle of incidence of 0° , to thereby form the p-type, source-and-drain regions 10b. Boron herein is also implanted into the gate electrode 6b. The dose of boron in this process is controlled to a smaller value ($3 \times 10^{15}/\text{cm}^2$, for example) than that in general formation process of p-type, source-and-drain regions.

Next, the resist mask 19 is removed typically by ashing, and the sidewalls 9a, 9b are dry-etched (over-etched) to thereby allow the upper portion of both side faces of the gate electrodes 6a, 6b to expose as much as 50 nm or around as shown in Fig. 7D. The gate electrodes 6a, 6b herein are remained so as to expose an area extending from the top surface thereof to the upper portion of both side faces thereof, and the sidewalls 9a, 9b are adjusted so as to have a height of 50 nm or around.

Considering now that the gate electrodes 6a, 6b are subjected to tilt-angled ion implantation described later, the more the sidewalls 9a, 9b are etched, the more the gate electrodes 6a, 6b will have an impurity incorporated therein. Too much amount of

etching of the sidewalls 9a, 9b may, however, result in excessive diffusion of the incorporated impurities in the source-and-drain regions 10a, 10b towards the channel, or may raise a risk of short-circuiting between silicides, which are formed later on the source-and-drain regions 10a, 10b and on the gate electrodes 6a, 6b. Thus there is an appropriate range for the amount of etching of the sidewalls 9a, 9b, and 50 nm is one exemplary amount falls within such range.

To prevent the STI-type element isolation structure 2 from being etched together with the sidewalls 9a, 9b, it is preferable to use different materials to form the sidewalls 9a, 9b and STI-type element isolation structure 2 so that the sidewalls 9a, 9b will have a higher etchrate than that of the element isolation structure 2. One preferable example is such that using a plasma oxide film formed in an HDP (high density plasma) apparatus for the STI-type element isolation structure 2 and using an oxide film formed using TEOS (tetraethoxysilane) for the sidewalls 9a, 9b.

Next, as shown in Fig. 8A, an n-type impurity is implanted along a direction inclined into the nMOS region 11 to thereby introduce the impurity to the exposed surface of the gate electrode 6a (the top surface of 50 nm wide and both side faces of 50 nm high exposed from the sidewall 9a).

More specifically, a resist mask 21 is formed so as to cover the pMOS region 12, and an n-type impurity, which is phosphorus (P) herein, is implanted at an ion acceleration energy of 4 keV, a dose of $5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times (twice in two opposing directions parallel to the gate length and twice in two opposing directions normal thereto). The ion implantation repeated four times is shown in a schematic plan view in Fig. 9.

Fig. 8A shows an exemplary ion implantation effected along a direction parallel to the gate length and at an angle of incidence of 45° . Since the top surface and the upper portion of one side face of the gate electrode 6a herein have almost equivalent exposed areas, a single ion implantation according to the above conditions results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6a in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice, and also results in introduction of the impurity into one n-type, source-and-drain region 10a in an amount equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° . Another n-type, source-and-drain region 10a, which is shadowed by the gate

electrode 6a, is not introduced with the impurity, or introduced only in a less affective amount.

Although not being illustrated for convenience, a single ion implantation normal to the gate length at an angle of incidence of 45° results in introduction of the impurity into the gate electrode 6a in an amount equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° , and also results in introduction of the impurity into both n-type, source-and-drain regions 10a in an amount again equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° .

By the aforementioned ion implantation repeated four times, as shown later in Table 1, the gate electrode 6a will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° ($5 \times 10^{14}/\text{cm}^2$) repeated six times, in addition to a dose of $4.5 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of phosphorus of $7.5 \times 10^{15}/\text{cm}^2$. On the contrary, each n-type, source-and-drain region 10a will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated three times, in addition to a dose of $4.5 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will

have a total dose of phosphorus of $6 \times 10^{15}/\text{cm}^2$ (same level with that of general source-and-drain region).

In the aforementioned process for forming the n-type, source-and-drain region 10a, the first ion implantation (at an angle of incidence of 0°) was carried out at an ion acceleration energy of 8 keV, whereas the successive tilt-angled ion implantation was carried at an ion acceleration energy reduced to as low as 4 keV. The energy was thus reduced because it was necessary to prevent the impurity from laterally penetrating the gate electrode 6a, to prevent the impurity from penetrating the sidewall 10a and gate electrode 6a and intruding into the semiconductor substrate 1, and to prevent the impurity implanted into the n-type, source-and-drain region 10a from diffusing toward the channel.

Next, as shown in Fig. 8B, a p-type impurity is implanted into the pMOS region 12 to thereby introduce the impurity to the exposed surface of the gate electrode 6b (the top surface of 50 nm wide and both side faces of 50 nm high exposed from the sidewall 9b).

More specifically, a resist mask 21 is removed typically by ashing, and a resist mask 22 is formed so as to cover the nMOS region 11, and a p-type impurity, which is boron (B) herein, is implanted at an ion acceleration energy of 2 keV, a dose of $2.5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The

implantation is repeated four times (twice in two opposing directions parallel to the gate length and twice in two opposing directions normal thereto).

Fig. 8B shows an exemplary ion implantation effected along a direction parallel to the gate length and at an angle of incidence of 45° . Since the top surface and the upper portion of one side face of the gate electrode 6b herein have almost equivalent exposed areas, a single ion implantation according to the above conditions results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6b in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice, and also results in introduction of the impurity into one p-type, source-and-drain region 10b in an amount equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° . Another p-type, source-and-drain region 10b, which is shadowed by the gate electrode 6b, is not introduced with the impurity, or introduced only in a less affective amount.

Although not being illustrated for convenience, a single ion implantation normal to the gate length at an angle of incidence of 45° results in introduction of the impurity into the gate electrode 6b in an amount equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° ,

and also results in introduction of the impurity into both p-type, source-and-drain regions 10b in an amount again equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° .

By the aforementioned ion implantation repeated four times, as shown later in Table 1, the gate electrode 6b will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° ($2.5 \times 10^{14}/\text{cm}^2$) repeated six times, in addition to a dose of $2.25 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of boron of $3.75 \times 10^{15}/\text{cm}^2$. On the contrary, each p-type, source-and-drain region 10b will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated three times, in addition to a dose of $2.25 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of boron of $3 \times 10^{15}/\text{cm}^2$ (same level with that of general source-and-drain region).

In the aforementioned process for forming the p-type, source-and-drain region 10b, the first ion implantation (at an angle of incidence of 0°) was carried out at an ion acceleration energy of 4 keV, whereas the successive tilt-angled ion implantation was carried at an ion acceleration energy reduced to

as low as 2 keV. The energy was thus reduced because it was necessary to prevent the impurity from laterally penetrating the gate electrode 6b, to prevent the impurity from penetrating the sidewall 10b and gate electrode 6b and intruding into the semiconductor substrate 1, and to prevent the impurity implanted into the p-type, source-and-drain region 10b from diffusing toward the channel.

Next, the resist mask 22 is removed typically by ashing, and, as shown in Fig. 8C, the semiconductor substrate 1 is then annealed by RTA (rapid thermal annealing) at 1,030°C for one second to thereby restore it from damage caused by ion implantation into the gate electrodes 6a, 6b and source-and-drain regions 10a, 10b, and to thereby activate the impurities.

Next, a silicide-forming metal, which is cobalt (Co) herein, is deposited over the entire surface, annealed so as to proceed silicidation, and unreacted Co is removed, to thereby form CoSi_2 layers 23 on the exposed surface of the gate electrodes 6a, 6b and on the surface of the source-and-drain region 10a, 10b as shown in Fig. 8D.

An interlayer insulating film 24 is deposited over the entire surface, wirings 26 are formed so as to make contact through contact holes 25, and a CMOS transistor is completed after some additional post-processes.

As has been described in the above, the first embodiment is successful in controlling the impurity concentration of the gate electrodes 6a, 6b higher than that of the source-and-drain regions 10a, 10b by forming the sidewalls 9a, 9a so as to expose the upper portion of the gate electrodes 6a, 6b, and by carrying out the ion implantation at an angle of incidence of 45°. In the first embodiment, the impurity concentration of the gate electrodes 6a, 6b becomes higher than that of the source-and-drain regions 10a, 10b by approx. 25%, where the impurity concentration of the gate electrodes 6a, 6b can be raised while keeping the general impurity concentration of the source-and-drain regions 10a, 10b unchanged. The present embodiment is thus to provide a highly-reliable CMOS transistor having an improved gate capacitance and short-channel resistance without anticipating fluctuation in the threshold voltage due to variation in shape of the gate electrode.

(Modified Example)

A modified example of the present embodiment will be described.

The present invention is by no means limited to mode of the ion implantation in the first embodiment described in the above, where conditions for the first ion implantation for forming the source-and-drain regions or successive tilt-angled ion

implantations can properly be selected provided that the impurity concentration of the gate electrodes can be raised without increasing the impurity concentration of the source-and-drain regions.

For example, in this modified example, as shown in Fig. 10, the first ion implantation of phosphorus for forming the n-type, source-and-drain region 10a is carried out at an ion acceleration energy of 8 keV, a dose of $5.5 \times 10^{15}/\text{cm}^2$ and an angle of incidence of 0° , and the tilt-angled ion implantation of phosphorus is carried out twice along the direction parallel to the gate length respectively at an ion acceleration energy of 4 keV, a dose of $5 \times 10^{14}/\text{cm}^2$ and an angle of incidence of 45° .

By the ion implantation repeated twice, as shown later in Table 1, the gate electrode 6a will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° ($5 \times 10^{14}/\text{cm}^2$) repeated four times, in addition to a dose of $5.5 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of phosphorus of $7.5 \times 10^{15}/\text{cm}^2$. On the contrary, each n-type, source-and-drain region 10a will have introduced therein the impurity in an amount equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° , in addition to a dose of $5.5 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will

have a total dose of phosphorus of $6 \times 10^{15}/\text{cm}^2$ (same level with that of general source-and-drain region).

Similarly to the above, the first ion implantation of boron for forming the p-type, source-and-drain region 10b is carried out at an ion acceleration energy of 4 keV, a dose of $2.75 \times 10^{15}/\text{cm}^2$ and an angle of incidence of 0° , and the tilt-angled ion implantation of phosphorus is carried out twice along the direction parallel to the gate length individually at an ion acceleration energy of 2 keV, a dose of $2.5 \times 10^{14}/\text{cm}^2$ and an angle of incidence of 45° .

By the ion implantation repeated twice, as shown later in Table 1, the gate electrode 6b will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° ($2.5 \times 10^{14}/\text{cm}^2$) repeated four times, in addition to a dose of $2.75 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of boron of $3.75 \times 10^{15}/\text{cm}^2$. On the contrary, each p-type, source-and-drain region 10b will have introduced therein the impurity in an amount equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° , in addition to a dose of $2.75 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of boron of $3 \times 10^{15}/\text{cm}^2$ (same level with that of general source-and-drain region).

(Second Embodiment)

Figs. 11A to 11D are schematic sectional views sequentially showing major process steps of a method of fabricating a CMOS transistor according to a second embodiment.

In the second embodiment, the individual process steps previously shown in Figs. 4A through 8B are executed to thereby control the dose of phosphorus to $7.5 \times 10^{15}/\text{cm}^2$ for the gate electrode 6a and $6 \times 10^{15}/\text{cm}^2$ for the n-type, source-and-drain region 10a in the nMOS region 11, and the dose of boron to $3.75 \times 10^{15}/\text{cm}^2$ for the gate electrode 6b and $3 \times 10^{15}/\text{cm}^2$ for the p-type, source-and-drain region 10b in the pMOS region 12. The semiconductor substrate 1 is then annealed by RTA at $1,030^\circ\text{C}$ for 1 second (Fig. 11A).

Next, as shown in Fig. 11B, a silicon oxide film 27 is formed over the entire surface by the CVD process, and then as shown in Fig. 11C, the silicon oxide film 27 is then anisotropically etched back so as to allow the film to remain only on both side faces of the gate electrodes 6a, 6b, to thereby form sidewalls 9a, 9b. That is, the sidewalls 9a, 9b now recover the status previously shown in Fig. 7A.

Next, a silicide-forming metal, which is cobalt (Co) herein, is deposited over the entire surface, annealed so as to proceed silicidation, and unreacted Co is removed, to thereby form CoSi_2 layers 23 on the exposed surface of the gate electrodes 6a, 6b and on

the surface of the source-and-drain region 10a, 10b as shown in Fig. 11D.

An interlayer insulating film 24 is deposited over the entire surface, wirings 26 are formed so as to make contact through contact holes 25, and a CMOS transistor is completed after some additional post-processes.

As has been described in the above, the second embodiment is successful in controlling the impurity concentration of the gate electrodes 6a, 6b higher than that of the source-and-drain regions 10a, 10b by forming the sidewalls 9a, 9a so as to expose the upper portion of the gate electrodes 6a, 6b, and by carrying out the ion implantation at an angle of incidence of 45° . In the second embodiment, the impurity concentration of the gate electrodes 6a, 6b becomes higher than that of the source-and-drain regions 10a, 10b by approx. 25%, where the impurity concentration of the gate electrodes 6a, 6b can be raised while keeping the general impurity concentration of the source-and-drain regions 10a, 10b unchanged. The present embodiment is thus to provide a highly-reliable CMOS transistor having an improved gate capacitance and short-channel resistance without anticipating fluctuation in the threshold voltage due to variation in shape of the gate electrode.

The second embodiment is also successful in certainly prevent short-circuiting between CoSi_2 formed on the source-and-drain regions 10a, 10b and CoSi_2 formed on the gate electrodes 6a, 6b, since the sidewalls 9a, 9b recover their initial form almost completely covering the side faces of the gate electrodes before the CoSi_2 layer 23 is formed. Thus the sidewalls 9a, 9b can thoroughly be over-etched in preparation for the tilt-angled ion implantation without anticipating the short-circuiting. It is therefore also preferable to raise the amount of over-etching larger than that in the first embodiment (50%), to thereby further increase dose of implanted ion in the gate electrodes 6a, 6b.

Also in the second embodiment, similarly to the modified example of the first embodiment, conditions for the first ion implantation for forming the source-and-drain regions or successive tilt-angled ion implantations can properly be selected provided that the impurity concentration of the gate electrodes can be raised without increasing the impurity concentration of the source-and-drain regions.

For example, the first ion implantation of phosphorus for forming the n-type, source-and-drain region 10a is carried out at an ion acceleration energy of 8 keV, a dose of $5.5 \times 10^{15}/\text{cm}^2$ and an angle of incidence of 0° , and the tilt-angled ion

implantation of phosphorus is carried out twice along the direction parallel to the gate length respectively at an ion acceleration energy of 4 keV, a dose of $5 \times 10^{14}/\text{cm}^2$ and an angle of incidence of 45° .

By the ion implantation repeated twice, as shown later in Table 1, the gate electrode 6a will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° ($5 \times 10^{14}/\text{cm}^2$) repeated four times, in addition to a dose of $5.5 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of phosphorus of $7.5 \times 10^{15}/\text{cm}^2$. On the contrary, each n-type, source-and-drain region 10a will have introduced therein the impurity in an amount equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° , in addition to a dose of $5.5 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of phosphorus of $6 \times 10^{15}/\text{cm}^2$ (same level with that of general source-and-drain region).

Similarly to the above, the first ion implantation of boron for forming the p-type, source-and-drain region 10b is carried out at an ion acceleration energy of 4 keV, a dose of $2.75 \times 10^{15}/\text{cm}^2$ and an angle of incidence of 0° , and the tilt-angled ion implantation of boron is carried out twice along the direction parallel to the gate length respectively at an ion acceleration energy of 2 keV,

a dose of $2.5 \times 10^{14}/\text{cm}^2$ and an angle of incidence of 45° .

By the ion implantation repeated twice, as shown later in Table 1, the gate electrode 6b will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° ($2.5 \times 10^{14}/\text{cm}^2$) repeated four times, in addition to a dose of $2.75 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of boron of $3.75 \times 10^{15}/\text{cm}^2$. On the contrary, each p-type, source-and-drain region 10b will have introduced therein the impurity in an amount equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° , in addition to a dose of $2.75 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of boron of $3 \times 10^{15}/\text{cm}^2$ (same level with that of general source-and-drain region).

(Third Embodiment)

Figs. 12A through 13D are schematic sectional views sequentially showing major process steps of a method of fabricating a CMOS transistor according to a third embodiment.

In the third embodiment, the individual process steps previously shown in Figs. 4A through 6B are executed to thereby form the sidewalls 9a, 9b which cover both side faces of the gate electrodes 6a, 6b

and having a maximum width of 80 nm or around (Fig. 12A).

Next, as shown in Fig. 12B, the resist mask 18 is formed so as to cover the pMOS region 12, and an n-type impurity, which is phosphorus (P) herein, is introduced by ion implantation into the nMOS region 11 at an ion acceleration energy of 8 keV, a dose of $5 \times 10^{15}/\text{cm}^2$, and an angle of incidence of 0° , to thereby form the n-type, source-and-drain regions 10a. Phosphorus herein is also implanted into the gate electrode 6a. The dose of phosphorus in this process is controlled to a smaller value ($6 \times 10^{15}/\text{cm}^2$, for example) than that in general formation process of n-type, source-and-drain regions.

Next, the resist mask 18 is removed typically by ashing, the resist mask 19 is formed so as to cover the nMOS region 11 as shown in Fig. 12C, and a p-type impurity, which is boron (B) herein, is introduced by ion implantation into the pMOS region 12 at an ion acceleration energy of 4 keV, a dose of $2.5 \times 10^{15}/\text{cm}^2$ and an angle of incidence of 0° , to thereby form the p-type, source-and-drain regions 10b. Boron herein is also implanted into the gate electrode 6b. The dose of boron in this process is controlled to a smaller value ($3 \times 10^{15}/\text{cm}^2$, for example) than that in general formation process of p-type, source-and-drain regions.

Next, the resist mask 19 is removed typically by ashing, and the sidewalls 9a, 9b are dry-etched (over-etched) to thereby allow the upper portion of both side faces of the gate electrodes 6a, 6b to expose as much as 50 nm or around as shown in Fig. 12D. The gate electrodes 6a, 6b herein are remained so as to expose an area extending from the top surface thereof to the upper portion of both side faces thereof, and the sidewalls 9a, 9b are adjusted so as to have a height of 50 nm or around.

Considering now that the gate electrodes 6a, 6b are subjected to tilt-angled ion implantation described later, the more the sidewalls 9a, 9b are etched, the more the gate electrodes 6a, 6b will have an impurity incorporated therein. Too much amount of etching of the sidewalls 9a, 9b may, however, result in excessive diffusion of the incorporated impurity in the source-and-drain regions 10a, 10b towards the channel, or may raise a risk of short-circuiting between silicides, which are formed later on the source-and-drain regions 10a, 10b and on the gate electrodes 6a, 6b. Thus there is an appropriate range for the amount of etching of the sidewalls 9a, 9b, and 50 nm is one exemplary amount falls within such range.

To prevent the STI-type element isolation structure 2 from being etched together with the sidewalls 9a, 9b, it is preferable to use different

materials to form the sidewalls 9a, 9b and STI-type element isolation structure 2 so that the sidewalls 9a, 9b will have a higher etchrate than that of the element isolation structure 2. One preferable example is such that using a plasma oxide film formed in an HDP (high density plasma) apparatus for the STI-type element isolation structure 2 and using an oxide film formed using TEOS (tetraethoxysilane) for the sidewalls 9a, 9b.

Next, as shown in Fig. 13A, an n-type impurity is implanted along a direction inclined into the nMOS region 11 to thereby introduce the impurity to the exposed surface of the gate electrode 6a (the top surface of 50 nm wide and both side faces of 50 nm high exposed from the sidewall 9a).

More specifically, the resist mask 21 is formed so as to cover the pMOS region 12, and an n-type impurity, which is phosphorus (P) herein, is implanted at an ion acceleration energy of 4 keV, a dose of $5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times from directions differing from each other (four different directions inclined by 45° away from the direction of gate length). The ion implantation repeated four times is shown in a schematic plan view in Fig. 14.

Since the top surface and the upper portion of one side face of the gate electrode 6a herein have almost equivalent exposed areas, a single ion

implantation according to the above conditions results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6a in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice, and also results in introduction of the impurity into one n-type, source-and-drain region 10a in an amount equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° . Another n-type, source-and-drain region 10a, which is shadowed by the gate electrode 6a, is not introduced with the impurity, or introduced only in a less effective amount.

By the aforementioned ion implantation repeated four times, as shown later in Table 1, the gate electrode 6a will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° ($5 \times 10^{14}/\text{cm}^2$) repeated eight times, in addition to a dose of $5 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of phosphorus of $9 \times 10^{15}/\text{cm}^2$. On the contrary, each n-type, source-and-drain region 10a will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice, in addition to a dose of $5 \times 10^{15}/\text{cm}^2$ which has

previously been attained, and thus will have a total dose of phosphorus of $6 \times 10^{15}/\text{cm}^2$ (same level with that of general source-and-drain region).

In the aforementioned process for forming the n-type, source-and-drain region 10a, the first ion implantation (at an angle of incidence of 0°) was carried out at an ion acceleration energy of 8 keV, whereas the successive tilt-angled ion implantation was carried at an ion acceleration energy reduced to as low as 4 keV. The energy was thus reduced because it was necessary to prevent the impurity from laterally penetrating the gate electrode 6a, to prevent the impurity from penetrating the sidewall 10a and gate electrode 6a and intruding into the semiconductor substrate 1, and to prevent the impurity implanted into the n-type, source-and-drain region 10a from diffusing toward the channel.

Next, as shown in Fig. 13B, a p-type impurity is implanted into the pMOS region 12 to thereby introduce the impurity to the exposed surface of the gate electrode 6b (the top surface of 50 nm wide and both side faces of 50 nm high exposed from the sidewall 9b).

More specifically, the resist mask 21 is removed typically by ashing, and the resist mask 22 is formed so as to cover the nMOS region 11, and a p-type impurity, which is boron (B) herein, is implanted at an ion acceleration energy of 2 keV, a dose of $2.5 \times$

$10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times from directions differing from each other (four different directions inclined by 45° away from the direction of gate length).

Since the top surface and the upper portion of one side face of the gate electrode 6b herein have almost equivalent exposed areas, a single ion implantation according to the above conditions results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6b in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice, and also results in introduction of the impurity into one p-type, source-and-drain region 10b in an amount equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° . Another p-type, source-and-drain region 10b, which is shadowed by the gate electrode 6b, is not introduced with the impurity, or introduced only in a less effective amount.

By the aforementioned ion implantation repeated four times, as shown later in Table 1, the gate electrode 6b will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° ($2.5 \times 10^{14}/\text{cm}^2$) repeated eight times,

in addition to a dose of $2.5 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of boron of $4.5 \times 10^{15}/\text{cm}^2$. On the contrary, each p-type, source-and-drain region 10b will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice, in addition to a dose of $2.5 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of boron of $3 \times 10^{15}/\text{cm}^2$ (same level with that of general source-and-drain region).

In the aforementioned process for forming the p-type, source-and-drain region 10b, the first ion implantation (at an angle of incidence of 0°) was carried out at an ion acceleration energy of 4 keV, whereas the successive tilt-angled ion implantation was carried at an ion acceleration energy reduced to as low as 2 keV. The energy was thus reduced because it was necessary to prevent the impurity from laterally penetrating the gate electrode 6b, to prevent the impurity from penetrating the sidewall 10b and gate electrode 6b and intruding into the semiconductor substrate 1, and to prevent the impurity implanted into the p-type, source-and-drain region 10b from diffusing toward the channel.

Next, the resist mask 22 is removed typically by ashing, and, as shown in Fig. 13C, the semiconductor substrate 1 is then annealed by RTA (rapid thermal

annealing) at 1,030°C for one second to thereby restore it from damage caused by ion implantation into the gate electrodes 6a, 6b and source-and-drain regions 10a, 10b, and to thereby activate the impurities.

Next, a silicide-forming metal, which is cobalt (Co) herein, is deposited over the entire surface, annealed so as to proceed silicidation, and unreacted Co is removed, to thereby form CoSi_2 layers 23 on the exposed surface of the gate electrodes 6a, 6b and on the surface of the source-and-drain region 10a, 10b as shown in Fig. 13D.

An interlayer insulating film 24 is deposited over the entire surface, wirings 26 are formed so as to make contact through contact holes 25, and a CMOS transistor is completed after some additional post-processes.

As has been described in the above, the third embodiment is successful in controlling the impurity concentration of the gate electrodes 6a, 6b higher than that of the source-and-drain regions 10a, 10b by forming the sidewalls 9a, 9a so as to expose the upper portion of the gate electrodes 6a, 6b, and by carrying out the ion implantation from four inclined directions at an angle of incidence of 45°. In the third embodiment, the impurity concentration of the gate electrodes 6a, 6b becomes higher than that of the source-and-drain regions 10a, 10b by approx. 50%,

where the impurity concentration of the gate electrodes 6a, 6b can be raised while keeping the general impurity concentration of the source-and-drain regions 10a, 10b unchanged. The third embodiment is thus to provide a highly-reliable CMOS transistor having an improved gate capacitance and short-channel resistance without anticipating fluctuation in the threshold voltage due to variation in shape of the gate electrode.

(Fourth Embodiment)

Figs. 15A through 16D are schematic sectional views sequentially showing major process steps of a method of fabricating a CMOS transistor according to a fourth embodiment.

In the fourth embodiment, the individual process steps previously shown in Figs. 4A through 6B are executed to thereby form the sidewalls 9a, 9b which cover both side faces of the gate electrodes 6a, 6b and having a maximum width of 80 nm or around (Fig. 15A).

Next, as shown in Fig. 15B, the resist mask 18 is formed so as to cover the pMOS region 12, and an n-type impurity, which is phosphorus (P) herein, is introduced by ion implantation into the nMOS region 11 at an ion acceleration energy of 8 keV, a dose of $5 \times 10^{15}/\text{cm}^2$, and an angle of incidence of 0° , to thereby form the n-type, source-and-drain regions 10a. Phosphorus herein is also implanted into the gate electrode 6a. The dose of phosphorus in this process

is controlled to a smaller value ($6 \times 10^{15}/\text{cm}^2$, for example) than that in general formation process of n-type, source-and-drain regions.

Next, the resist mask 18 is removed typically by ashing, the resist mask 19 is formed so as to cover the nMOS region 11 as shown in Fig. 15C, and a p-type impurity, which is boron (B) herein, is introduced by ion implantation into the pMOS region 12 at an ion acceleration energy of 4 keV, a dose of $2.5 \times 10^{15}/\text{cm}^2$ and an angle of incidence of 0° , to thereby form the p-type, source-and-drain regions 10b. Boron herein is also implanted into the gate electrode 6b. The dose of boron in this process is controlled to a smaller value ($3 \times 10^{15}/\text{cm}^2$, for example) than that in general formation process of p-type, source-and-drain regions.

Next, the resist mask 19 is removed typically by ashing, and the sidewalls 9a, 9b are dry-etched (over-etched) to thereby allow the upper portion of both side faces of the gate electrodes 6a, 6b to expose as much as 50 nm or around as shown in Fig. 15D. The gate electrodes 6a, 6b herein are remained so as to expose an area extending from the top surface thereof to the upper portion of both side faces thereof, and the sidewalls 9a, 9b are adjusted so as to have a height of 50 nm or around.

Considering now that the gate electrodes 6a, 6b are subjected to tilt-angled ion implantation

described later, the more the sidewalls 9a, 9b are etched, the more the gate electrodes 6a, 6b will have an impurity incorporated therein. Too much amount of etching of the sidewalls 9a, 9b may, however, result in excessive diffusion of the incorporated impurity in the source-and-drain regions 10a, 10b towards the channel, or may raise a risk of short-circuiting between silicides, which are formed later on the source-and-drain regions 10a, 10b and on the gate electrodes 6a, 6b. Thus there is an appropriate range for the amount of etching of the sidewalls 9a, 9b, and 50 nm is one exemplary amount falls within such range.

To prevent the STI-type element isolation structure 2 from being etched together with the sidewalls 9a, 9b, it is preferable to use different materials to form the sidewalls 9a, 9b and STI-type element isolation structure 2 so that the sidewalls 9a, 9b will have a higher etchrate than that of the element isolation structure 2. One preferable example is such that using a plasma oxide film formed in an HDP (high density plasma) apparatus for the STI-type element isolation structure 2 and using an oxide film formed using TEOS (tetraethoxysilane) for the sidewalls 9a, 9b.

Next, as shown in Fig. 16A, an n-type impurity is implanted along a direction inclined into the nMOS region 11 to thereby introduce the impurity to the

exposed surface of the gate electrode 6a (the top surface of 50 nm wide and both side faces of 50 nm high exposed from the sidewall 9a).

More specifically, a resist mask 31 is formed so as to cover the pMOS region 12, which mask 31 having an opening 31a formed in a size capable of protecting the n-type, source-and-drain regions 10a from the tilt-angled ion implantation. The resist mask 31 herein is approx. 120 nm high, and the opening 31a has an edge 120 nm away from the edge of the gate electrode 6a. In alignment of a reticle for forming the opening 31a by photolithography, employing the gate electrode as an alignment mark, in place of a mark formed in the STI process, can successfully reduce mis-alignment. An n-type impurity, which is phosphorus (P) herein, is implanted into the nMOS region 11 at an ion acceleration energy of 4 keV, a dose of $5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times from four directions differing from each other (twice in two opposing directions parallel to the gate length and twice in two opposing directions normal thereto). The ion implantation repeated four times is shown in a schematic plan view in Fig. 17.

Fig. 16A shows an exemplary ion implantation effected along a direction parallel to the gate length and at an angle of incidence of 45° . Since the top surface and the upper portion of one side face of

the gate electrode 6a herein have almost equivalent exposed areas, a single ion implantation according to the above conditions results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6a in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice. On the other hand, a pair of n-type, source-and-drain regions 10a are protected by the resist mask 31 against the ion implantation, and are thus prevented from being implanted with the impurity.

Although not being illustrated for convenience, a single ion implantation normal to the gate length at an angle of incidence of 45° results in introduction of the impurity into the gate electrode 6a in an amount equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° , and also results in introduction of the impurity into both n-type, source-and-drain regions 10a in an amount again equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° .

By the aforementioned ion implantation repeated four times, as shown later in Table 1, the gate electrode 6a will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of

incidence of 0° ($5 \times 10^{14}/\text{cm}^2$) repeated six times, in addition to a dose of $5 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of phosphorus of $8 \times 10^{15}/\text{cm}^2$. On the contrary, each n-type, source-and-drain region 10a will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice, in addition to a dose of $5 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of phosphorus of $6 \times 10^{15}/\text{cm}^2$ (same level with that of general source-and-drain region).

In the aforementioned process for forming the n-type, source-and-drain region 10a, the first ion implantation (at an angle of incidence of 0°) was carried out at an ion acceleration energy of 8 keV, whereas the successive tilt-angled ion implantation was carried at an ion acceleration energy reduced to as low as 4 keV. The energy was thus reduced because it was necessary to prevent the impurity from laterally penetrating the gate electrode 6a, to prevent the impurity from penetrating the sidewall 10a and gate electrode 6a and intruding into the semiconductor substrate 1, and to prevent the impurity implanted into the n-type, source-and-drain region 10a from diffusing toward the channel.

Next, as shown in Fig. 16B, a p-type impurity is implanted along a direction inclined into the pMOS

region 12 to thereby introduce the impurity to the exposed surface of the gate electrode 6b (the top surface of 50 nm wide and both side faces of 50 nm high exposed from the sidewall 9b).

More specifically, the resist mask 31 is removed typically by ashing, and a resist mask 32 is formed so as to cover the nMOS region 11, which mask 32 having an opening 32a formed in a size capable of protecting the p-type, source-and-drain regions 10b from the tilt-angled ion implantation. The resist mask 32 herein is approx. 120 nm high, and the opening 32a has an edge 120 nm away from the edge of the gate electrode 6b. In alignment of a reticle for forming the opening 31a by photolithography, employing the gate electrode as an alignment mark, in place of a mark formed in the STI process, can successfully reduce mis-alignment. A p-type impurity, which is boron (B) herein, is implanted into the pMOS region 12 at an ion acceleration energy of 2 keV, a dose of $2.5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times from four directions differing from each other (twice in two opposing directions parallel to the gate length and twice in two opposing directions normal thereto).

Fig. 16B shows an exemplary ion implantation effected along a direction parallel to the gate length and at an angle of incidence of 45° . Since the top surface and the upper portion of one side face of

the gate electrode 6b herein have almost equivalent exposed areas, a single ion implantation according to the above conditions results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6b in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice. On the other hand, a pair of p-type, source-and-drain regions 10b are protected by the resist mask 32 against the ion implantation, and are thus prevented from being implanted with the impurity.

Although not being illustrated for convenience, a single ion implantation normal to the gate length at an angle of incidence of 45° results in introduction of the impurity into the gate electrode 6b in an amount equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° , and also results in introduction of the impurity into both p-type, source-and-drain regions 10b in an amount again equivalent to that possibly attained by a single ion implantation at an angle of incidence of 0° .

By the aforementioned ion implantation repeated four times, as shown later in Table 1, the gate electrode 6b will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of

incidence of 0° ($2.5 \times 10^{14}/\text{cm}^2$) repeated six times, in addition to a dose of $2.5 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of boron of $4 \times 10^{15}/\text{cm}^2$. On the contrary, each p-type, source-and-drain region 10b will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice, in addition to a dose of $2.5 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of boron of $3 \times 10^{15}/\text{cm}^2$ (same level with that of general source-and-drain region).

In the aforementioned process for forming the p-type, source-and-drain region 10b, the first ion implantation (at an angle of incidence of 0°) was carried out at an ion acceleration energy of 4 keV, whereas the successive tilt-angled ion implantation was carried at an ion acceleration energy reduced to as low as 2 keV. The energy was thus reduced because it was necessary to prevent the impurity from laterally penetrating the gate electrode 6b, to prevent the impurity from penetrating the sidewall 10b and gate electrode 6b and intruding into the semiconductor substrate 1, and to prevent the impurity implanted into the p-type, source-and-drain region 10b from diffusing toward the channel.

Next, the resist mask 32 is removed typically by ashing, and, as shown in Fig. 16C, the semiconductor

substrate 1 is then annealed by RTA (rapid thermal annealing) at 1,030°C for one second to thereby restore it from damage caused by ion implantation into the gate electrodes 6a, 6b and source-and-drain regions 10a, 10b, and to thereby activate the impurities.

Next, a silicide-forming metal, which is cobalt (Co) herein, is deposited over the entire surface, annealed so as to proceed silicidation, and unreacted Co is removed, to thereby form CoSi_2 layers 23 on the exposed surface of the gate electrodes 6a, 6b and on the surface of the source-and-drain region 10a, 10b as shown in Fig. 16D.

An interlayer insulating film 24 is deposited over the entire surface, wirings 26 are formed so as to make contact through contact holes 25, and a CMOS transistor is completed after some additional post-processes.

As has been described in the above, the fourth embodiment is successful in controlling the impurity concentration of the gate electrodes 6a, 6b higher than that of the source-and-drain regions 10a, 10b by forming the sidewalls 9a, 9a so as to expose the upper portion of the gate electrodes 6a, 6b, and by carrying out the ion implantation from four inclined directions at an angle of incidence of 45°. In the fourth embodiment, the impurity concentration of the gate electrodes 6a, 6b becomes higher than that of

the source-and-drain regions 10a, 10b by approx. 33%, where the impurity concentration of the gate electrodes 6a, 6b can be raised while keeping the general impurity concentration of the source-and-drain regions 10a, 10b unchanged. The fourth embodiment is thus to provide a highly-reliable CMOS transistor having an improved gate capacitance and short-channel resistance without anticipating fluctuation in the threshold voltage due to variation in shape of the gate electrode.

Moreover in the tilt-angled ion implantation, the source-and-drain regions 10a, 10b are successfully prevented from being implanted with the impurities by virtue of the resist masks 31, 32, and only the gate electrodes 6a, 6b are implanted with impurity ions. This strongly ensures the gate electrodes 6a, 6b to have a higher impurity concentration than the source-and-drain regions 10a, 10b have.

(Modified Example)

Also in the fourth embodiment, similarly to the modified example of the first embodiment, conditions for the first ion implantation for forming the source-and-drain regions or successive tilt-angled ion implantations can properly be selected provided that the impurity concentration of the gate electrodes can be raised without increasing the impurity concentration of the source-and-drain regions.

For example, the first ion implantation of phosphorus for forming the n-type, source-and-drain region 10a is carried out at an ion acceleration energy of 8 keV, a dose of $6 \times 10^{15}/\text{cm}^2$ and an angle of incidence of 0° , and the tilt-angled ion implantation of phosphorus is carried out twice along the direction parallel to the gate length respectively at an ion acceleration energy of 4 keV, a dose of $5 \times 10^{14}/\text{cm}^2$ and an angle of incidence of 45° .

By the ion implantation repeated twice, as shown later in Table 1, the gate electrode 6a will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° ($5 \times 10^{14}/\text{cm}^2$) repeated four times, in addition to a dose of $6 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of phosphorus of $8 \times 10^{15}/\text{cm}^2$. On the contrary, each n-type, source-and-drain region 10a will contain the impurity only in an amount of $6 \times 10^{15}/\text{cm}^2$ which has initially been attained, which will be at the same level with that of general source-and-drain region.

Similarly to the above, the first ion implantation of boron for forming the p-type, source-and-drain region 10b is carried out at an ion acceleration energy of 4 keV, a dose of $3 \times 10^{15}/\text{cm}^2$ and an angle of incidence of 0° , and the tilt-angled ion implantation of boron is carried out twice along the

direction parallel to the gate length respectively at an ion acceleration energy of 2 keV, a dose of $2.5 \times 10^{14}/\text{cm}^2$ and an angle of incidence of 45° .

By the ion implantation repeated twice, as shown later in Table 1, the gate electrode 6b will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° ($2.5 \times 10^{14}/\text{cm}^2$) repeated four times, in addition to a dose of $3 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of boron of $4 \times 10^{15}/\text{cm}^2$. On the contrary, each p-type, source-and-drain region 10b will contain the impurity only in an amount of $3 \times 10^{15}/\text{cm}^2$ which has initially been attained, which will be at the same level with that of general source-and-drain region.

(Fifth Embodiment)

Figs. 18A through 19D are schematic sectional views sequentially showing major process steps of a method of fabricating a CMOS transistor according to a fifth embodiment.

In the fifth embodiment, the individual process steps previously shown in Figs. 4A through 6B are executed to thereby form the sidewalls 9a, 9b which cover both side faces of the gate electrodes 6a, 6b and having a maximum width of 80 nm or around (Fig. 18A).

Next, as shown in Fig. 18B, the resist mask 18 is

formed so as to cover the pMOS region 12, and an n-type impurity, which is phosphorus (P) herein, is introduced by ion implantation into the nMOS region 11 at an ion acceleration energy of 8 keV, a dose of $6 \times 10^{15}/\text{cm}^2$, and an angle of incidence of 0° , to thereby form the n-type, source-and-drain regions 10a. Phosphorus herein is also implanted into the gate electrode 6a.

Next, the resist mask 18 is removed typically by ashing, the resist mask 19 is formed so as to cover the nMOS region 11 as shown in Fig. 18C, and a p-type impurity, which is boron (B) herein, is introduced by ion implantation into the pMOS region 12 at an ion acceleration energy of 4 keV, a dose of $3 \times 10^{15}/\text{cm}^2$ and an angle of incidence of 0° , to thereby form the p-type, source-and-drain regions 10b. Boron herein is also implanted into the gate electrode 6b.

Next, the resist mask 19 is removed typically by ashing, and the sidewalls 9a, 9b are dry-etched (over-etched) to thereby allow the upper portion of both side faces of the gate electrodes 6a, 6b to expose as much as 50 nm or around as shown in Fig. 18D. The gate electrodes 6a, 6b herein are remained so as to expose an area extending from the top surface thereof to the upper portion of both side faces thereof, and the sidewalls 9a, 9b are adjusted so as to have a height of 50 nm or around.

Considering now that the gate electrodes 6a, 6b are subjected to tilt-angled ion implantation described later, the more the sidewalls 9a, 9b are etched, the more the gate electrodes 6a, 6b will have an impurity incorporated therein. Too much amount of etching of the sidewalls 9a, 9b may, however, result in excessive diffusion of the incorporated impurity in the source-and-drain regions 10a, 10b towards the channel, or may raise a risk of short-circuiting between silicides, which are formed later on the source-and-drain regions 10a, 10b and on the gate electrodes 6a, 6b. Thus there is an appropriate range for the amount of etching of the sidewalls 9a, 9b, and 50 nm is one exemplary amount falls within such range.

To prevent the STI-type element isolation structure 2 from being etched together with the sidewalls 9a, 9b, it is preferable to use different materials to form the sidewalls 9a, 9b and STI-type element isolation structure 2 so that the sidewalls 9a, 9b will have a higher etchrate than that of the element isolation structure 2. One preferable example is such that using a plasma oxide film formed in an HDP (high density plasma) apparatus for the STI-type element isolation structure 2 and using an oxide film formed using TEOS (tetraethoxysilane) for the sidewalls 9a, 9b.

Next, as shown in Fig. 19A, an n-type impurity is implanted along a direction inclined into the nMOS region 11 to thereby introduce the impurity to the exposed surface of the gate electrode 6a (the top surface of 50 nm wide and both side faces of 50 nm high exposed from the sidewall 9a).

More specifically, a resist mask 33 is formed so as to cover the pMOS region 12, which mask 33 having an opening 33a formed in a size capable of protecting the n-type, source-and-drain regions 10a from the tilt-angled ion implantation. The resist mask 33 herein is approx. 120 nm high, and the opening 33a has an edge 120 nm away from the edge of the gate electrode 6a. In alignment of a reticle for forming the opening 33a by photolithography, employing the gate electrode as an alignment mark, in place of a mark formed in the STI process, can successfully reduce mis-alignment. An n-type impurity, which is phosphorus (P) herein, is implanted into the nMOS region 11 at an ion acceleration energy of 4 keV, a dose of $5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times from directions differing from each other (four different directions inclined by 45° away from the direction of gate length). The ion implantation repeated four times is shown in a schematic plan view in Fig. 20.

A single ion implantation according to the above conditions results in introduction of the impurity

over the area extending from the top surface to the upper portion of one side face of the gate electrode 6a in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice. On the other hand, a pair of n-type, source-and-drain regions 10a are protected by the resist mask 33 against the ion implantation, and are thus prevented from being implanted with the impurity.

By the aforementioned ion implantation repeated four times, as shown later in Table 1, the gate electrode 6a will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° ($5 \times 10^{14}/\text{cm}^2$) repeated eight times, in addition to a dose of $6 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of phosphorus of $1 \times 10^{16}/\text{cm}^2$. On the contrary, each n-type, source-and-drain region 10a will contain the impurity only in an amount of $6 \times 10^{15}/\text{cm}^2$ which has initially been attained, which will be at the same level with that of general source-and-drain region.

In the aforementioned process for forming the n-type, source-and-drain region 10a, the first ion implantation (at an angle of incidence of 0°) was carried out at an ion acceleration energy of 8 keV, whereas the successive tilt-angled ion implantation was carried at an ion acceleration energy reduced to as low as 4 keV. The energy was thus reduced because

it was necessary to prevent the impurity from laterally penetrating the gate electrode 6a, to prevent the impurity from penetrating the sidewall 10a and gate electrode 6a and intruding into the semiconductor substrate 1, and to prevent the impurity implanted into the n-type, source-and-drain region 10a from diffusing toward the channel.

Next, as shown in Fig. 19B, a p-type impurity is implanted into the pMOS region 12 to thereby introduce the impurity to the exposed surface of the gate electrode 6b (the top surface of 50 nm wide and both side faces of 50 nm high exposed from the sidewall 9b).

More specifically, the resist mask 33 is removed typically by ashing, and a resist mask 34 is formed so as to cover the nMOS region 11, which mask 34 having an opening 34a formed in a size capable of protecting the p-type, source-and-drain regions 10b from the tilt-angled ion implantation. The resist mask 34 herein is approx. 120 nm high, and the opening 34a has an edge 120 nm away from the edge of the gate electrode 6b. In alignment of a reticle for forming the opening 31a by photolithography, employing the gate electrode as an alignment mark, in place of a mark formed in the STI process, can successfully reduce mis-alignment. A p-type impurity, which is boron (B) herein, is implanted into the pMOS region 12 at an ion acceleration energy of 2 keV, a

dose of $2.5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times from directions differing from each other (four different directions inclined by 45° away from the direction of gate length).

A single ion implantation according to the above conditions results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6b in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice. On the other hand, a pair of p-type, source-and-drain regions 10b are protected by the resist mask 34 against the ion implantation, and are thus prevented from being implanted with the impurity.

By the aforementioned ion implantation repeated four times, as shown later in Table 1, the gate electrode 6b will have introduced therein the impurity in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° ($2.5 \times 10^{14}/\text{cm}^2$) repeated eight times, in addition to a dose of $3 \times 10^{15}/\text{cm}^2$ which has previously been attained, and thus will have a total dose of boron of $5 \times 10^{15}/\text{cm}^2$. On the contrary, each p-type, source-and-drain region 10b will contain the impurity only in an amount of $3 \times 10^{15}/\text{cm}^2$ which has initially been attained, which will be at the same level with that of general source-and-drain region.

In the aforementioned process for forming the p-type, source-and-drain region 10b, the first ion implantation (at an angle of incidence of 0°) was carried out at an ion acceleration energy of 4 keV, whereas the successive tilt-angled ion implantation was carried at an ion acceleration energy reduced to as low as 2 keV. The energy was thus reduced because it was necessary to prevent the impurity from laterally penetrating the gate electrode 6b, to prevent the impurity from penetrating the sidewall 10b and gate electrode 6b and intruding into the semiconductor substrate 1, and to prevent the impurity implanted into the n-type, source-and-drain region 10b from diffusing toward the channel.

Next, the resist mask 34 is removed typically by ashing, and, as shown in Fig. 19C, the semiconductor substrate 1 is then annealed by RTA (rapid thermal annealing) at $1,030^\circ\text{C}$ for one second to thereby restore it from damage caused by ion implantation into the gate electrodes 6a, 6b and source-and-drain regions 10a, 10b, and to thereby activate the impurities.

Next, a silicide-forming metal, which is cobalt (Co) herein, is deposited over the entire surface, annealed so as to proceed silicidation, and unreacted Co is removed, to thereby form CoSi_2 layers 23 on the exposed surface of the gate electrodes 6a, 6b and on

the surface of the source-and-drain region 10a, 10b as shown in Fig. 19D.

An interlayer insulating film 24 is deposited over the entire surface, wirings 26 are formed so as to make contact through contact holes 25, and a CMOS transistor is completed after some additional post-processes.

As has been described in the above, the fifth embodiment is successful in controlling the impurity concentration of the gate electrodes 6a, 6b higher than that of the source-and-drain regions 10a, 10b by forming the sidewalls 9a, 9a so as to expose the upper portion of the gate electrodes 6a, 6b, and by carrying out the ion implantation from four inclined directions at an angle of incidence of 45° . In the fifth embodiment, the impurity concentration of the gate electrodes 6a, 6b becomes higher than that of the source-and-drain regions 10a, 10b by approx. 66%, where the impurity concentration of the gate electrodes 6a, 6b can be raised while keeping the general impurity concentration of the source-and-drain regions 10a, 10b unchanged. The fifth embodiment is thus to provide a highly-reliable CMOS transistor having an improved gate capacitance and short-channel resistance without anticipating fluctuation in the threshold voltage due to variation in shape of the gate electrode.

In addition, the source-and-drain regions 10a, 10b are successfully prevented from being implanted with the impurities by virtue of the resist masks 33, 34, and only the gate electrodes 6a, 6b are implanted with impurity ions. This strongly ensures the gate electrodes 6a, 6b to have a higher impurity concentration than the source-and-drain regions 10a, 10b have.

Short-circuiting between the silicides formed on the source-and-drain regions 10a, 10b and the silicides formed on the gate electrodes 6a, 6b can be prevented by combining the fifth embodiment and second embodiment. This desirably increases the amount of etching of the sidewalls 9a, 9b than that in the fifth embodiment, and makes it possible to further increase the dose of impurities incorporated into the gate electrodes 6a, 6b. It is even allowable to completely remove the sidewalls 9a, 9b by over-etching, because the introduction of impurities into the source-and-drain regions 10a, 10b can be prevented by the resist masks 33, 34 even in the absence of the sidewalls 9a, 9b.

(Sixth Embodiment)

Figs. 21A through 23D are schematic sectional views sequentially showing major process steps of a method of fabricating a CMOS transistor according to a sixth embodiment.

In the sixth embodiment, the individual process steps previously shown in Figs. 4A through 5C are executed similarly to as described in the first embodiment, to thereby pattern the gate electrodes 6a, 6b (Fig. 21A).

Next, as shown in Fig. 21B, an n-type impurity is implanted along a direction inclined into the nMOS region 11 to thereby introduce the impurity to the exposed surface of the gate electrode 6a (the top surface of 50 nm wide).

More specifically, a resist mask 35 is formed so as to cover the pMOS region 12, which mask 35 having an opening 35a formed in a size capable of protecting the n-type, source-and-drain regions 10a from the tilt-angled ion implantation. The resist mask 35 herein is approx. 120 nm high, and the opening 35a has an edge 80 nm away from the edge of the gate electrode 6a. In alignment of a reticle for forming the opening 35a by photolithography, employing the gate electrode as an alignment mark, in place of a mark formed in the STI process, can successfully reduce mis-alignment. An n-type impurity, which is phosphorus (P) herein, is implanted into the nMOS region 11 at an ion acceleration energy of 4 keV, a dose of $5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times from directions differing from each other (four different directions inclined by 45° away from the direction of

gate length). The ion implantation repeated four times is shown in a schematic plan view in Fig. 24.

Since the top surface and the upper portion of one side face of the gate electrode 6a herein have almost equivalent exposed areas, a single ion implantation according to the above conditions results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6a in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice. On the other hand, a pair of n-type, source-and-drain regions 10a are protected by the resist mask 35 against the ion implantation, and are thus prevented from being implanted with the impurity.

Next, as shown in Fig. 21C, a p-type impurity is implanted along a direction inclined into the pMOS region 12 to thereby introduce the impurity to the exposed surface of the gate electrode 6b (the top surface of 50 nm wide).

More specifically, the resist mask 35 is removed typically by ashing, and a resist mask 36 is formed so as to cover the nMOS region 11, which mask 36 having an opening 36a formed in a size capable of protecting the p-type, source-and-drain regions 10b from the tilt-angled ion implantation. The resist mask 36 herein is approx. 120 nm high, and the opening 36a has an edge 80 nm away from the edge of

the gate electrode 6b. In alignment of a reticle for forming the opening 36a by photolithography, employing the gate electrode as an alignment mark, in place of a mark formed in the STI process, can successfully reduce mis-alignment. A p-type impurity, which is boron (B) herein, is implanted into the pMOS region 12 at an ion acceleration energy of 2 keV, a dose of $2.5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times from directions differing from each other (four different directions inclined by 45° away from the direction of gate length).

A single ion implantation according to the above conditions results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6b in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice. On the other hand, a pair of p-type, source-and-drain regions 10b are protected by the resist mask 36 against the ion implantation, and are thus prevented from being implanted with the impurity.

Next, the resist mask 36 is removed typically by ashing, the resist mask 16 is formed so as to cover the pMOS region 12 as shown in Fig. 21D, and an n-type impurity, which is arsenic (As) herein, is introduced by vertical ion implantation into the nMOS region 11 at an ion acceleration energy of 5 keV and

a dose of $6 \times 10^{14}/\text{cm}^2$; and a p-type impurity, which is boron (B) herein, is also introduced by ion implantation at an ion acceleration energy of 10 keV, a dose of $8 \times 10^{12}/\text{cm}^2$ and at an angle of incidence of 30° from four directions to thereby form n-type extension layers 7a and p-type pocket layers 8a, respectively.

Next, the resist mask 16 is removed typically by ashing, the resist mask 17 is formed so as to cover the nMOS region 11 as shown in Fig. 22A, and a p-type impurity, which is boron (B) herein, is introduced by vertical ion implantation into the pMOS region 12 at an ion acceleration energy of 0.5 keV and a dose of $6 \times 10^{14}/\text{cm}^2$; and an n-type impurity, which is arsenic (As) herein, is also introduced by ion implantation at an ion acceleration energy of 50 keV, a dose of $6 \times 10^{12}/\text{cm}^2$ and at an angle of incidence of 30° from four directions to thereby form p-type extension layers 7b and n-type pocket layers 8b, respectively.

It is to be noted now that the individual process steps shown in Figs. 21B through 22A can be executed in an arbitrary order.

Next, the resist mask 17 is removed typically by ashing, and, as shown in Fig. 22B, the semiconductor substrate 1 is then annealed by RTA (rapid thermal annealing) at $1,000^\circ\text{C}$ for one second to thereby restore it from damage caused by the ion implantation

into the extension layers 7a, 7b and pocket layers 8a, 8b.

Next, a silicon oxide film (not shown) is deposited on the entire surface by the CVD process, and the film is then anisotropically etched back so as to allow the film to remain only on both side faces of the gate electrodes 6a, 6b, to thereby form sidewalls 20a, 20b having a maximum width of 80 nm or around, as shown in Fig. 22C.

Next, a resist mask 18 is formed so as to cover the pMOS region 12 as shown in Fig. 22D, and an n-type impurity, which is phosphorus (P) herein, is introduced by ion implantation into the nMOS region 11 at an ion acceleration energy of 8 keV, a dose of $6 \times 10^{15}/\text{cm}^2$, and an angle of incidence of 0° (that is, normal to the surface of the substrate), to thereby form the n-type, source-and-drain regions 10a. Phosphorus herein is also implanted into the gate electrode 6a.

In this case, the gate electrode 6a is subjected to four times of the aforementioned tilt-angled ion implantation and a single ion implantation at an angle of incidence of 0° , which results in introduction of the impurity in an amount equivalent to eight times of $5 \times 10^{14}/\text{cm}^2$ plus $6 \times 10^{15}/\text{cm}^2$, total $1 \times 10^{16}/\text{cm}^2$ of phosphorus. On the contrary, each n-type, source-and-drain region 10a will have introduced therein the impurity only in an amount of $6 \times 10^{15}/\text{cm}^2$,

which will be at the same level with that of general source-and-drain region.

Next, a resist mask 18 is removed typically by ashing, and the resist mask 19 is formed so as to cover the nMOS region 11 as shown in Fig. 23A, and a p-type impurity, which is boron (B) herein, is introduced by ion implantation into the pMOS region 12 at an ion acceleration energy of 4 keV, a dose of $3 \times 10^{15}/\text{cm}^2$, and an angle of incidence of 0° , to thereby form the p-type, source-and-drain regions 10b. Boron herein is also implanted into the gate electrode 6b.

In this case, the gate electrode 6b is subjected to four times of the aforementioned tilt-angled ion implantation and a single ion implantation at an angle of incidence of 0° , which results in introduction of the impurity in an amount equivalent to eight times of $2.5 \times 10^{14}/\text{cm}^2$ plus $3 \times 10^{15}/\text{cm}^2$, total $5 \times 10^{15}/\text{cm}^2$ of boron. On the contrary, each p-type, source-and-drain region 10b will have introduced therein the impurity only in an amount of $3 \times 10^{15}/\text{cm}^2$, which will be at the same level with that of general source-and-drain region.

Next, the resist mask 19 is removed typically by ashing, and, as shown in Fig. 23B, the semiconductor substrate 1 is then annealed by RTA (rapid thermal annealing) at $1,030^\circ\text{C}$ for one second to thereby restore it from damage caused by ion implantation

into the gate electrodes 6a, 6b and source-and-drain regions 10a, 10b, and to thereby activate the impurities.

Next, a silicide-forming metal, which is cobalt (Co) herein, is deposited over the entire surface, annealed so as to proceed silicidation, and unreacted Co is removed, to thereby form CoSi_2 layers 23 on the exposed surface of the gate electrodes 6a, 6b and on the surface of the source-and-drain region 10a, 10b as shown in Fig. 23C.

An interlayer insulating film 24 is deposited over the entire surface, wirings 26 are formed so as to make contact through contact holes 25, and a CMOS transistor is completed after some additional post-processes as shown in Fig. 23D.

As has been described in the above, the sixth embodiment is successful in controlling the impurity concentration of the gate electrodes 6a, 6b higher than that of the source-and-drain regions 10a, 10b by carrying out the ion implantation from four inclined directions at an angle of incidence of 45° . In the sixth embodiment, the impurity concentration of the gate electrodes 6a, 6b becomes higher than that of the source-and-drain regions 10a, 10b by approx. 66%, where the impurity concentration of the gate electrodes 6a, 6b can be raised while keeping the general impurity concentration of the source-and-drain regions 10a, 10b unchanged. The sixth

embodiment is thus to provide a highly-reliable CMOS transistor having an improved gate capacitance and short-channel resistance without anticipating fluctuation in the threshold voltage due to variation in shape of the gate electrode.

Moreover, in the tilt-angled ion implantation, the source-and-drain regions 10a, 10b are successfully prevented from being implanted with the impurities by virtue of the resist masks 35, 36, and only the gate electrodes 6a, 6b are implanted with impurity ions. This strongly ensures the gate electrodes 6a, 6b to have a higher impurity concentration than the source-and-drain regions 10a, 10b have.

The sixth embodiment is also advantageous in reducing the production cost of CMOS transistor, since a process step of thinning the sidewalls 20a, 20b by over-etching is omissible, although the amounts of dose of impurities in the source-and-drain regions 10a, 10b and gate electrodes 6a, 6b are attainable at the same level with those in the fifth embodiment.

(Seventh Embodiment)

Figs. 25A through 27D are schematic sectional views sequentially showing major process steps of a method of fabricating a CMOS transistor according to a seventh embodiment.

In the sixth embodiment, the individual process steps previously shown in Figs. 4A through 5C are executed similarly to as described in the first embodiment, to thereby pattern the gate electrodes 6a, 6b.

Next, as shown in Fig. 25A, an n-type impurity is implanted along a direction inclined into the nMOS region 11 to thereby introduce the impurity to the exposed surface of the gate electrode 6a (the top surface of 50 nm wide).

More specifically, a resist mask 37 is formed so as to cover the pMOS region 12, which mask 37 having an opening 37a formed in a size capable of protecting the n-type, source-and-drain regions 10a from the tilt-angled ion implantation. The resist mask 37 herein is approx. 120 nm high, and the opening 37a has an edge 80 nm away from the edge of the gate electrode 6a. In alignment of a reticle for forming the opening 37a by photolithography, employing the gate electrode as an alignment mark, in place of a mark formed in the STI process, can successfully reduce mis-alignment. An n-type impurity, which is phosphorus (P) herein, is implanted into the nMOS region 11 at an ion acceleration energy of 4 keV, a dose of $5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times from directions differing from each other (four different

directions inclined by 45° away from the direction of gate length).

Since the top surface and the upper portion of one side face of the gate electrode 6a herein have almost equivalent exposed areas, a single ion implantation according to the above conditions results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6a in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice. On the other hand, a pair of n-type, source-and-drain regions 10a are protected by the resist mask 37 against the ion implantation, and are thus prevented from being implanted with the impurity.

Next, as shown in Fig. 25B, in the presence of the resist mask 37 remained unremoved, an n-type impurity, which is arsenic (As) herein, is vertically implanted into the nMOS region 11 at an ion acceleration energy of 5 keV and a dose of $6 \times 10^{14}/\text{cm}^2$; and a p-type impurity, which is boron (B) herein, is also introduced by ion implantation at an ion acceleration energy of 10 keV, a dose of $8 \times 10^{12}/\text{cm}^2$ and at an angle of incidence of 15° from four directions to thereby form n-type extension layers 7a and p-type pocket layers 8a, respectively.

Next, as shown in Fig. 25C, a p-type impurity is implanted along a direction inclined into the pMOS

region 12 to thereby introduce the impurity to the exposed surface of the gate electrode 6b (the top surface of 50 nm wide).

More specifically, the resist mask 37 is removed typically by ashing, and a resist mask 38 is formed so as to cover the nMOS region 11, which mask 38 having an opening 38a formed in a size capable of protecting the p-type, source-and-drain regions 10b from the tilt-angled ion implantation. The resist mask 38 herein is approx. 120 nm high, and the opening 38a has an edge 80 nm away from the edge of the gate electrode 6b. In alignment of a reticle for forming the opening 38a by photolithography, employing the gate electrode as an alignment mark, in place of a mark formed in the STI process, can successfully reduce mis-alignment. A p-type impurity, which is boron (B) herein, is implanted into the pMOS region 12 at an ion acceleration energy of 2 keV, a dose of $2.5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times from directions differing from each other (four different directions inclined by 45° away from the direction of gate length).

A single ion implantation according to the above conditions results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6b in an amount equivalent to that possibly attained

by ion implantations at an angle of incidence of 0° repeated twice. On the other hand, a pair of p-type, source-and-drain regions 10b are protected by the resist mask 38 against the ion implantation, and are thus prevented from being implanted with the impurity.

Next, as shown in Fig. 25D, in the presence of the resist mask 38 remained unremoved, a p-type impurity, which is boron (B) herein, is vertically implanted into the pMOS region 12 at an ion acceleration energy of 0.5 keV and a dose of $6 \times 10^{14}/\text{cm}^2$; and an n-type impurity, which is arsenic (As) herein, is also introduced by ion implantation at an ion acceleration energy of 50 keV, a dose of $6 \times 10^{12}/\text{cm}^2$ and at an angle of incidence of 15° from four directions to thereby form p-type extension layers 7b and n-type pocket layers 8b, respectively.

Next, the resist mask 38 is removed typically by ashing, and, as shown in Fig. 26A, the semiconductor substrate 1 is then annealed by RTA (rapid thermal annealing) at $1,000^\circ\text{C}$ for one second to thereby restore it from damage caused by the ion implantation into the extension layers 7a, 7b and pocket layers 8a, 8b.

Next, a silicon oxide film (not shown) is deposited on the entire surface by the CVD process, and the film is then anisotropically etched back so as to allow the film to remain only on both side faces of the gate electrodes 6a, 6b, to thereby form

sidewalls 9a, 9b having a maximum width of 80 nm or around, as shown in Fig. 26B.

Next, a resist mask 18 is formed so as to cover the pMOS region 12 as shown in Fig. 26C, and an n-type impurity, which is phosphorus (P) herein, is introduced by ion implantation into the nMOS region 11 at an ion acceleration energy of 8 keV, a dose of $6 \times 10^{15}/\text{cm}^2$, and an angle of incidence of 0° (that is, normal to the surface of the substrate), to thereby form the n-type, source-and-drain regions 10a. Phosphorus herein is also implanted into the gate electrode 6a.

In this case, the gate electrode 6a is subjected to four times of the aforementioned tilt-angled ion implantation and a single ion implantation at an angle of incidence of 0° , which results in introduction of the impurity in an amount equivalent to eight times of $5 \times 10^{14}/\text{cm}^2$ plus $6 \times 10^{15}/\text{cm}^2$, total $1 \times 10^{16}/\text{cm}^2$ of phosphorus. On the contrary, each n-type, source-and-drain region 10a will have introduced therein the impurity only in an amount of $6 \times 10^{15}/\text{cm}^2$, which will be at the same level with that of general source-and-drain region.

Next, a resist mask 18 is removed typically by ashing, and the resist mask 19 is formed so as to cover the nMOS region 11 as shown in Fig. 26D, and a p-type impurity, which is boron (B) herein, is introduced by ion implantation into the pMOS region 12 at an ion acceleration energy of 4 keV, a dose of

$3 \times 10^{15}/\text{cm}^2$, and an angle of incidence of 0° , to thereby form the p-type, source-and-drain regions 10b. Boron herein is also implanted into the gate electrode 6b.

In this case, the gate electrode 6b is subjected to four times of the aforementioned tilt-angled ion implantation and a single ion implantation at an angle of incidence of 0° , which results in introduction of the impurity in an amount equivalent to eight times of $2.5 \times 10^{14}/\text{cm}^2$ plus $3 \times 10^{15}/\text{cm}^2$, total $5 \times 10^{15}/\text{cm}^2$ of boron. On the contrary, each p-type, source-and-drain region 10b will have introduced therein the impurity only in an amount of $3 \times 10^{15}/\text{cm}^2$, which will be at the same level with that of general source-and-drain region.

Next, the resist mask 19 is removed typically by ashing, and, as shown in Fig. 27A, the semiconductor substrate 1 is then annealed by RTA (rapid thermal annealing) at $1,030^\circ\text{C}$ for one second to thereby restore it from damage caused by ion implantation into the gate electrodes 6a, 6b and source-and-drain regions 10a, 10b, and to thereby activate the impurities.

Next, a silicide-forming metal, which is cobalt (Co) herein, is deposited over the entire surface, annealed so as to proceed silicidation, and unreacted Co is removed, to thereby form CoSi_2 layers 23 on the exposed surface of the gate electrodes 6a, 6b and on

the surface of the source-and-drain region 10a, 10b as shown in Fig. 27B.

An interlayer insulating film 24 is deposited over the entire surface, wirings 26 are formed so as to make contact through contact holes 25, and a CMOS transistor is completed after some additional post-processes as shown in Fig. 27C.

As has been described in the above, the seventh embodiment is successful in controlling the impurity concentration of the gate electrodes 6a, 6b higher than that of the source-and-drain regions 10a, 10b by carrying out the ion implantation from four inclined directions at an angle of incidence of 45° . In the seventh embodiment, the impurity concentration of the gate electrodes 6a, 6b becomes higher than that of the source-and-drain regions 10a, 10b by approx. 66%, where the impurity concentration of the gate electrodes 6a, 6b can be raised while keeping the general impurity concentration of the source-and-drain regions 10a, 10b unchanged. The seventh embodiment is thus to provide a highly-reliable CMOS transistor having an improved gate capacitance and short-channel resistance without anticipating fluctuation in the threshold voltage due to variation in shape of the gate electrode.

Moreover, in the tilt-angled ion implantation, the source-and-drain regions 10a, 10b are successfully prevented from being implanted with the

impurities by virtue of the resist masks 37, 38, and only the gate electrodes 6a, 6b are implanted with impurity ions. This strongly ensures the gate electrodes 6a, 6b to have a higher impurity concentration than the source-and-drain regions 10a, 10b have.

The seventh embodiment is also advantageous in further reducing the production cost of CMOS transistor, since a process step of thinning the sidewalls 20a, 20b by over-etching is omissible, and since a process step of photolithography for forming the extension layers 7a, 7b and pocket layers 8a, 8b is omissible, although the amounts of dose of impurities in the source-and-drain regions 10a, 10b and gate electrodes 6a, 6b are attainable at the same level with those in the fifth embodiment.

(Modified Example)

A modified example of the seventh embodiment will be described.

Figs. 28A through 29C are schematic sectional views sequentially showing major process steps of a method of fabricating a CMOS transistor according to a modified example of the seventh embodiment.

In this modified example, similarly to as previously shown in Fig. 25B, the gate electrode 6a is subjected to the tilt-angled ion implantation in the presence of the resist mask 37 (Fig. 28A).

Next, as shown in Fig. 28B, the resist mask 37 is trimmed so that the opening 37a is widened to have an edge recessed by 100 nm from the edge of the gate electrode 6a.

In this status, as shown in Fig. 28C, an n-type impurity, which is arsenic (As) herein, is vertically implanted into the nMOS region 11 at an ion acceleration energy of 5 keV and a dose of $6 \times 10^{14}/\text{cm}^2$; and a p-type impurity, which is boron (B) herein, is also introduced by ion implantation at an ion acceleration energy of 10 keV, a dose of $8 \times 10^{12}/\text{cm}^2$ and at an angle of incidence of 30° from four directions to thereby form the n-type extension layers 7a and p-type pocket layers 8a, respectively.

Next, the resist mask 37 is removed typically by ashing, and then similarly to as previously shown in Fig. 25C, the gate electrode 6b is subjected to the tilt-angled ion implantation in the presence of the resist mask 38 (Fig. 29A).

Next, as shown in Fig. 29B, the resist mask 38 is trimmed so that the opening 38a is widened to have an edge recessed by 100 nm from the edge of the gate electrode 6b.

In this status, a p-type impurity, which is boron (B) herein, is vertically implanted into the pMOS region 12 at an ion acceleration energy of 0.5 keV and a dose of $6 \times 10^{14}/\text{cm}^2$; and an n-type impurity, which is arsenic (As) herein, is also introduced by

ion implantation at an ion acceleration energy of 50 keV, a dose of $6 \times 10^{12}/\text{cm}^2$ and at an angle of incidence of 30° from four directions to thereby form the p-type extension layers 7b and n-type pocket layers 8b, respectively.

The resist mask 38 is then removed typically by ashing, and a CMOS transistor is completed after executing various process steps similarly to those in the seventh embodiment as shown in Figs. 26A to 27C.

In addition to various effects obtainable from the seventh embodiment, this modified example makes it possible to form the extension layers 7a, 7b and pocket layers 8a, 8b expanded to desired dimensions at a high degree of freedom by trimming the resist masks 37, 38, without limiting dimensions of the extension layers 7a, 7b and pocket layers 8a, 8b in view of preventing the tilt-angled ion implantation.

(Eighth Embodiment)

Figs. 30A through 32D are schematic sectional views sequentially showing major process steps of a method of fabricating a CMOS transistor according to a eighth embodiment.

In the eighth embodiment, the individual process steps previously shown in Figs. 4A through 5C are executed similarly to as described in the first embodiment, to thereby pattern the gate electrodes 6a, 6b (Fig. 30A).

Next, as shown in Fig. 30B, an n-type impurity is implanted along a direction inclined into the nMOS region 11 to thereby introduce the impurity to the exposed surface of the gate electrode 6a (the top surface of 50 nm wide).

More specifically, the resist mask 35 is formed so as to cover the pMOS region 12, which mask 35 having the opening 35a formed in a size capable of protecting the n-type, source-and-drain regions 10a from the tilt-angled ion implantation. The resist mask 35 herein is approx. 120 nm high, and the opening 35a has an edge 80 nm away from the edge of the gate electrode 6a. In alignment of a reticle for forming the opening 35a by photolithography, employing the gate electrode as an alignment mark, in place of a mark formed in the STI process, can successfully reduce mis-alignment. An n-type impurity, which is phosphorus (P) herein, is implanted into the nMOS region 11 at an ion acceleration energy of 4 keV, a dose of $5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times from directions differing from each other (four different directions inclined by 45° away from the direction of gate length).

Since the top surface and the upper portion of one side face of the gate electrode 6a herein have almost equivalent exposed areas, a single ion implantation according to the above conditions

results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6a in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice. On the other hand, a pair of n-type, source-and-drain regions 10a are protected by the resist mask 35 against the ion implantation, and are thus prevented from being implanted with the impurity.

Next, as shown in Fig. 30C, a p-type impurity is implanted along a direction inclined into the pMOS region 12 to thereby introduce the impurity to the exposed surface of the gate electrode 6b (the top surface of 50 nm wide).

More specifically, the resist mask 35 is removed typically by ashing, and the resist mask 36 is formed so as to cover the nMOS region 11, which mask 36 having the opening 36a formed in a size capable of protecting the p-type, source-and-drain regions 10b from the tilt-angled ion implantation. The resist mask 36 herein is approx. 120 nm high, and the opening 36a has an edge 80 nm away from the edge of the gate electrode 6b. In alignment of a reticle for forming the opening 36a by photolithography, employing the gate electrode as an alignment mark, in place of a mark formed in the STI process, can successfully reduce mis-alignment. A p-type impurity, which is boron (B) herein, is implanted into the pMOS

region 12 at an ion acceleration energy of 2 keV, a dose of $2.5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times from directions differing from each other (four different directions inclined by 45° away from the direction of gate length).

A single ion implantation according to the above conditions results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6b in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice. On the other hand, a pair of p-type, source-and-drain regions 10b are protected by the resist mask 36 against the ion implantation, and are thus prevented from being implanted with the impurity.

Next, the resist mask 36 is removed typically by ashing, and, as shown in Fig. 30D, the semiconductor substrate 1 is then annealed by RTA (rapid thermal annealing) at $1,050^\circ\text{C}$ for 1 second to thereby thoroughly diffuse the impurities incorporated into the gate electrodes 6a, 6b.

Next, the resist mask 16 is formed so as to cover the pMOS region 12 as shown in Fig. 31A, and an n-type impurity, which is arsenic (As) herein, is introduced by vertical ion implantation into the nMOS region 11 at an ion acceleration energy of 5 keV and a dose of $6 \times 10^{14}/\text{cm}^2$; and a p-type impurity, which is

boron (B) herein, is also introduced by ion implantation at an ion acceleration energy of 10 keV, a dose of $8 \times 10^{12}/\text{cm}^2$ and at an angle of incidence of 30° from four directions to thereby form the n-type extension layers 7a and p-type pocket layers 8a, respectively.

Next, the resist mask 16 is removed typically by ashing, the resist mask 17 is formed so as to cover the nMOS region 11 as shown in Fig. 31B, and a p-type impurity, which is boron (B) herein, is introduced by vertical ion implantation into the pMOS region 12 at an ion acceleration energy of 0.5 keV and a dose of $6 \times 10^{14}/\text{cm}^2$; and an n-type impurity, which is arsenic (As) herein, is also introduced by ion implantation at an ion acceleration energy of 50 keV, a dose of $6 \times 10^{12}/\text{cm}^2$ and at an angle of incidence of 30° from four directions to thereby form the p-type extension layers 7b and n-type pocket layers 8b, respectively.

Next, the resist mask 17 is removed typically by ashing, and, as shown in Fig. 31C, the semiconductor substrate 1 is then annealed by RTA (rapid thermal annealing) at $1,000^\circ\text{C}$ for one second to thereby restore it from damage caused by the ion implantation into the extension layers 7a, 7b and pocket layers 8a, 8b.

Next, a silicon oxide film (not shown) is deposited on the entire surface by the CVD process, and the film is then anisotropically etched back so

as to allow the film to remain only on both side faces of the gate electrodes 6a, 6b, to thereby form sidewalls 9a, 9b having a maximum width of 80 nm or around, as shown in Fig. 31D.

Next, a resist mask 18 is formed so as to cover the pMOS region 12 as shown in Fig. 32A, and an n-type impurity, which is phosphorus (P) herein, is introduced by ion implantation into the nMOS region 11 at an ion acceleration energy of 8 keV, a dose of $6 \times 10^{15}/\text{cm}^2$, and an angle of incidence of 0° (that is, normal to the surface of the substrate), to thereby form the n-type, source-and-drain regions 10a. Phosphorus herein is also implanted into the gate electrode 6a.

In this case, the gate electrode 6a is subjected to four times of the aforementioned tilt-angled ion implantation and a single ion implantation at an angle of incidence of 0° , which results in introduction of the impurity in an amount equivalent to eight times of $5 \times 10^{14}/\text{cm}^2$ plus $6 \times 10^{15}/\text{cm}^2$, total $1 \times 10^{16}/\text{cm}^2$ of phosphorus. On the contrary, each n-type, source-and-drain region 10a will have introduced therein the impurity only in an amount of $6 \times 10^{15}/\text{cm}^2$, which will be at the same level with that of general source-and-drain region.

Next, a resist mask 18 is removed typically by ashing, and the resist mask 19 is formed so as to cover the nMOS region 11 as shown in Fig. 32B, and a p-type impurity, which is boron (B) herein, is

introduced by ion implantation into the pMOS region 12 at an ion acceleration energy of 4 keV, a dose of $3 \times 10^{15}/\text{cm}^2$, and an angle of incidence of 0° , to thereby form the p-type, source-and-drain regions 10b. Boron herein is also implanted into the gate electrode 6b.

In this case, the gate electrode 6b is subjected to four times of the aforementioned tilt-angled ion implantation and a single ion implantation at an angle of incidence of 0° , which results in introduction of the impurity in an amount equivalent to eight times of $2.5 \times 10^{14}/\text{cm}^2$ plus $3 \times 10^{15}/\text{cm}^2$, total $5 \times 10^{15}/\text{cm}^2$ of boron. On the contrary, each p-type, source-and-drain region 10b will have introduced therein the impurity only in an amount of $3 \times 10^{15}/\text{cm}^2$, which will be at the same level with that of general source-and-drain region.

Next, the resist mask 19 is removed typically by ashing, and, as shown in Fig. 32C, the semiconductor substrate 1 is then annealed by RTA (rapid thermal annealing) at $1,020^\circ\text{C}$ for one second to thereby restore it from damage caused by ion implantation into the gate electrodes 6a, 6b and source-and-drain regions 10a, 10b, and to thereby activate the impurities. As described in the above, annealing temperature herein in the eighth embodiment can be reduced from $1,030^\circ\text{C}$ to $1,020^\circ\text{C}$ since the impurities introduced into the gate electrode 6a, 6b have

already been activated in the process step shown in Fig. 30D, which is advantageous in further suppressing diffusion of the impurities in the extension layers 7a, 7b and pocket layers 8a, 8b, and thus suppressing the short-channel effect.

Next, a silicide-forming metal, which is cobalt (Co) herein, is deposited over the entire surface, annealed so as to proceed silicidation, and unreacted Co is removed, to thereby form CoSi_2 layers 23 on the exposed surface of the gate electrodes 6a, 6b and on the surface of the source-and-drain region 10a, 10b as shown in Fig. 32D.

An interlayer insulating film 24 is deposited over the entire surface, wirings 26 are formed so as to make contact through contact holes 25, and a CMOS transistor is completed after some additional post-processes.

As has been described in the above, the eighth embodiment is successful in controlling the impurity concentration of the gate electrodes 6a, 6b higher than that of the source-and-drain regions 10a, 10b by carrying out the ion implantation from four inclined directions at an angle of incidence of 45° . In the eighth embodiment, the impurity concentration of the gate electrodes 6a, 6b becomes higher than that of the source-and-drain regions 10a, 10b by approx. 66%, where the impurity concentration of the gate electrodes 6a, 6b can be raised while keeping the

general impurity concentration of the source-and-drain regions 10a, 10b unchanged. The eighth embodiment is thus to provide a highly-reliable CMOS transistor having an improved gate capacitance and short-channel resistance without anticipating fluctuation in the threshold voltage due to variation in shape of the gate electrode.

Moreover, in the tilt-angled ion implantation, the source-and-drain regions 10a, 10b are successfully prevented from being implanted with the impurities by virtue of the resist masks 35, 36, and only the gate electrodes 6a, 6b are implanted with impurity ions. This strongly ensures the gate electrodes 6a, 6b to have a higher impurity concentration than the source-and-drain regions 10a, 10b have.

The eighth embodiment is also advantageous in reducing the production cost of CMOS transistor, since a process step of thinning the sidewalls 20a, 20b by over-etching is omissible, although the amounts of dose of impurities in the source-and-drain regions 10a, 10b and gate electrodes 6a, 6b are attainable at the same level with those in the fifth embodiment. Still another advantage resides in that the impurity concentration of the gate electrodes 6a, 6b can be raised in the vicinity of the gate insulating film 5, since the semiconductor substrate 1 is once annealed immediately after the gate

electrodes 6a, 6b are subjected to the tilt-angled ion implantation.

(Ninth Embodiment)

Figs. 33A through 34C are schematic sectional views sequentially showing major process steps of a method of fabricating a CMOS transistor according to a ninth embodiment.

In the ninth embodiment, the individual process steps previously shown in Figs. 4A through 5C are executed similarly to as described in the first embodiment, to thereby pattern the gate electrodes 6a, 6b (Fig. 33A).

Next, as shown in Fig. 33B, an n-type impurity is implanted along a direction inclined into the nMOS region 11 to thereby introduce the impurity to the exposed surface of the gate electrode 6a (the top surface of 50 nm wide).

More specifically, the resist mask 35 is formed so as to cover the pMOS region 12, which mask 35 having the opening 35a formed in a size capable of protecting the n-type, source-and-drain regions 10a from the tilt-angled ion implantation. The resist mask 35 herein is approx. 120 nm high, and the opening 35a has an edge 80 nm away from the edge of the gate electrode 6a. In alignment of a reticle for forming the opening 35a by photolithography, employing the gate electrode as an alignment mark, in place of a mark formed in the STI process, can

successfully reduce mis-alignment. An n-type impurity, which is phosphorus (P) herein, is implanted into the nMOS region 11 at an ion acceleration energy of 4 keV, a dose of $5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times from directions differing from each other (four different directions inclined by 45° away from the direction of gate length).

Since the top surface and the upper portion of one side face of the gate electrode 6a herein have almost equivalent exposed areas, a single ion implantation according to the above conditions results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6a in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice. On the other hand, a pair of n-type, source-and-drain regions 10a are protected by the resist mask 35 against the ion implantation, and are thus prevented from being implanted with the impurity.

Next, as shown in Fig. 33C, a p-type impurity is implanted along a direction inclined into the pMOS region 12 to thereby introduce the impurity to the exposed surface of the gate electrode 6b (the top surface of 50 nm wide).

More specifically, the resist mask 35 is removed typically by ashing, and the resist mask 36 is formed

so as to cover the nMOS region 11, which mask 36 having the opening 36a formed in a size capable of protecting the p-type, source-and-drain regions 10b from the tilt-angled ion implantation. The resist mask 36 herein is approx. 120 nm high, and the opening 36a has an edge 80 nm away from the edge of the gate electrode 6b. In alignment of a reticle for forming the opening 36a by photolithography, employing the gate electrode as an alignment mark, in place of a mark formed in the STI process, can successfully reduce mis-alignment. A p-type impurity, which is boron (B) herein, is implanted into the pMOS region 12 at an ion acceleration energy of 2 keV, a dose of $2.5 \times 10^{14}/\text{cm}^2$, and an angle of incidence of 45° . The implantation is repeated four times from directions differing from each other (four different directions inclined by 45° away from the direction of gate length).

A single ion implantation according to the above conditions results in introduction of the impurity over the area extending from the top surface to the upper portion of one side face of the gate electrode 6b in an amount equivalent to that possibly attained by ion implantations at an angle of incidence of 0° repeated twice. On the other hand, a pair of p-type, source-and-drain regions 10b are protected by the resist mask 36 against the ion implantation, and are thus prevented from being implanted with the impurity.

Next, the resist mask 36 is removed typically by ashing, and, as shown in Fig. 33D, a resist mask 41 is formed so as to cover the pMOS region 12, and an n-type impurity, which is phosphorus (P) herein, is introduced by ion implantation into the nMOS region 11 at an ion acceleration energy of 8 keV and a dose of $6 \times 10^{15}/\text{cm}^2$, to thereby form n-type, source-and-drain regions 43a.

Next, the resist mask 41 is removed typically by ashing, and, as shown in Fig. 34A, a resist mask 42 is formed so as to cover the nMOS region 11, and an p-type impurity, which is boron (B) herein, is introduced by ion implantation into the pMOS region 12 at an ion acceleration energy of 4 keV and a dose of $3 \times 10^{15}/\text{cm}^2$, to thereby form p-type, source-and-drain regions 43b.

Next, the resist mask 42 is removed typically by ashing, and, as shown in Fig. 34B, the semiconductor substrate 1 is then annealed by RTA (rapid thermal annealing) at $1,030^\circ\text{C}$ for 1 second to thereby thoroughly activate the impurities incorporated into the gate electrodes 6a, 6b and the source-and-drain regions 43a, 43b.

An interlayer insulating film 24 is deposited over the entire surface, wirings 26 are formed so as to make contact through contact holes 25, and a CMOS transistor is completed after some additional post-processes.

As has been described in the above, the ninth embodiment is successful in controlling the impurity concentration of the gate electrodes 6a, 6b higher than that of the source-and-drain regions 10a, 10b by carrying out the ion implantation from four inclined directions at an angle of incidence of 45° . In the ninth embodiment, the impurity concentration of the gate electrodes 6a, 6b can be raised without altering the general impurity concentration of the source-and-drain regions 10a, 10b. The ninth embodiment is thus to provide a highly-reliable CMOS transistor having an improved gate capacitance and short-channel resistance without anticipating fluctuation in the threshold voltage due to variation in shape of the gate electrode, by a less number of process steps.

Moreover, in the tilt-angled ion implantation, the source-and-drain regions 10a, 10b are successfully prevented from being implanted with the impurities by virtue of the resist masks 35, 36, and only the gate electrodes 6a, 6b are implanted with impurity ions. This strongly ensures the gate electrodes 6a, 6b to have a higher impurity concentration than the source-and-drain regions 10a, 10b have.

The amount of dose in the gate electrodes and source-and-drain regions according to the first through ninth embodiments are now listed in Table 1 below.

[Table 1]

	nMOS		pMOS	
	Dose in gate	Dose in S/D	Dose in gate	Dose in S/D
Prior art	6×10^{15} (1/cm ²)	6×10^{15}	3×10^{15}	3×10^{15}
1st embodiment	7.5×10^{15} (1a)	6×10^{15} (1b)	3.75×10^{15} (1c)	3×10^{15} (1d)
Modified example	7.5×10^{15} (2a)	6×10^{15} (2b)	3.75×10^{15} (2c)	3×10^{15} (2d)
3rd embodiment	9×10^{15} (3a)	6×10^{15} (3b)	4.5×10^{15} (3c)	3×10^{15} (3d)
4th embodiment	8×10^{15} (4a)	6×10^{15} (4b)	4×10^{15} (4c)	3×10^{15} (4d)
Modified example	8×10^{15} (5a)	6×10^{15} (5b)	4×10^{15} (5c)	3×10^{15} (5d)
5th embodiment	1×10^{16} (6a)	6×10^{15} (6b)	5×10^{15} (6c)	3×10^{15} (6d)

$$(1a) \quad 4.5 \times 10^{15} + 5 \times 10^{14} \times 6$$

$$(2a) \quad 5.5 \times 10^{15} + 5 \times 10^{14} \times 4$$

$$(3a) \quad 5 \times 10^{15} + 5 \times 10^{14} \times 8$$

$$(4a) \quad 5 \times 10^{15} + 5 \times 10^{14} \times 6$$

$$(5a) \quad 6 \times 10^{15} + 5 \times 10^{14} \times 4$$

$$(6a) \quad 6 \times 10^{15} + 5 \times 10^{14} \times 8$$

$$(1b) \quad 4.5 \times 10^{15} + 5 \times 10^{14} \times 3$$

$$(2b) \quad 5.5 \times 10^{15} + 5 \times 10^{14} \times 1$$

$$(3b) \quad 5 \times 10^{15} + 5 \times 10^{14} \times 2$$

$$(4b) \quad 5 \times 10^{15} + 5 \times 10^{14} \times 2$$

$$(5b) \quad 6 \times 10^{15}$$

$$(6b) \quad 6 \times 10^{15}$$

$$(1c) \quad 2.25 \times 10^{15} + 2.5 \times 10^{14} \times 6$$

$$(2c) \quad 2.75 \times 10^{15} + 2.5 \times 10^{14} \times 4$$

$$(3c) \quad 2.5 \times 10^{15} + 2.5 \times 10^{14} \times 8$$

$$(4c) \quad 2.5 \times 10^{15} + 2.5 \times 10^{14} \times 6$$

$$(5c) \quad 3 \times 10^{15} + 2.5 \times 10^{14} \times 4$$

$$(6c) \quad 3 \times 10^{15} + 2.5 \times 10^{14} \times 8$$

$$(1d) \quad 2.25 \times 10^{15} + 2.5 \times 10^{14} \times 3$$

$$(1d) \quad 2.75 \times 10^{15} + 2.5 \times 10^{14} \times 1$$

$$(1d) \quad 2.5 \times 10^{15} + 2.5 \times 10^{14} \times 2$$

$$(1d) \quad 2.5 \times 10^{15} + 2.5 \times 10^{14} \times 2$$

$$(1d) \quad 3 \times 10^{15}$$

$$(1d) \quad 3 \times 10^{15}$$

- Specific Alignment Conditions for Resist Mask and Gate Electrode Suitable for Tilt-angled Ion Implantation -

Next paragraphs will describe alignment rules for the resist mask for the tilt-angled ion implantation, and alignment rules for the gate electrode taking the tilt-angled ion implantation into account, which are applicable to the fourth through ninth embodiments.

[Fourth and Fifth Embodiments]

Fig. 35 shows a method of determining an alignment rule of a resist masks 31 through 34 with respect to the gate electrodes 6a, 6b (simply referred to as "gate electrode", hereinafter), which is applicable to the fourth and fifth embodiments. $Rp1$ represents the length of the sidewalls 9a, 9b (simply referred to as "sidewall" hereinafter) sufficient for shielding impurity implanted along direction inclined, and $Rp2$ represents the length of the resist mask sufficient for shielding impurity implanted along direction inclined.

First, $L1'$ is determined so that the projection range of the impurity implanted along a direction inclined in the sidewall will be longer than $Rp1$ based on the shape of the over-etched sidewall. Next, $L1''$ is determined so that the projection range of the impurity implanted along a direction inclined in the resist mask will be longer than $Rp2$. $L1'$ and $L1''$ are then compared, the shorter one of which is defined as $L1$, and a rule for the distance between the gate electrode and resist mask can be given as $L1 - \Delta L$, where ΔL is an alignment error between the gate electrode and resist pattern.

Figs. 36 and 37 show a method of determining an alignment rule for the case with aligned gate electrodes in the fourth and fifth embodiments.

Rp3 herein represents the length of the gate electrode sufficient for shielding impurity implanted along direction inclined.

First, $L2'$ is determined so that the projection range of the impurity implanted along a direction inclined in the over-etched sidewall will be longer than Rp1 based on the shape of the over-etched sidewall. Next, $L2'''$ is determined so as to allow the projection range of the impurity implanted along a direction inclined in the gate electrode impurity will be longer than Rp3. $L2'$ and $L2'''$ are then compared, and the shorter one of which is defined as $L2$. Assuming now a minimum formable width of a resist pattern 111 as $L3$. If the distance between the adjacent gate electrodes is longer than $2(L1 - \Delta L) + L3$, the resist pattern 111 can be formed between the adjacent gate electrodes according to the rule shown in Fig. 37.

On the other hand, if the distance between the adjacent gate electrodes is shorter than $2(L1 - \Delta L) + L3$ but longer than $L2$, it is necessary to fill the space between the adjacent gate electrodes with a resist pattern 111 having a width of $L3$. If the distance between the adjacent gate electrodes is shorter than $L2$, there is no need to form the resist pattern 111 between the adjacent gate electrodes.

[Sixth through Ninth Embodiments]

Fig. 38 shows a method of determining an alignment rule of a resist masks 35 through 38, 41 and 42 with respect to the gate electrode, which is applicable to the sixth through ninth embodiments. $Rp2$ represents the length of the resist mask sufficient for shielding impurity implanted along direction inclined, and $Rp3$ represents the length of the gate electrode sufficient for shielding impurity implanted along direction inclined.

First, $L1''$ is determined so that the projection range of the impurity implanted along a direction inclined in the resist mask will be longer than $Rp2$. Next, $L1'''$ is determined so that the projection range of the impurity implanted along a direction inclined in the gate electrode will be longer than $Rp3$. $L1''$ and $L1'''$ are then compared, the shorter one of which is defined as $L1$, and a rule for the distance between the gate electrode and resist mask can be given as $L1 - \Delta L$, where ΔL is an alignment error between the gate electrode and resist pattern.

Figs. 39 and 40 show a method of determining a rule for the case with aligned gate electrodes in the sixth through ninth embodiments. $Rp3$ herein represents the length of the gate electrode sufficient for shielding impurity implanted along direction inclined.

First, $L2$ is determined so that the projection range of the impurity implanted along a direction

inclined in the gate electrode will be longer than $Rp3$. If the distance between the adjacent gate electrodes is longer than $2(L1-\Delta L)+L3$, the resist pattern 111 as a part of the resist mask can be formed between the adjacent gate electrodes according to the rule shown in Fig. 40, where $L3$ is a minimum formable width of the resist pattern 111.

On the other hand, if the distance between the adjacent gate electrodes is shorter than $2(L1-\Delta L)+L3$ but longer than $L2$, it is necessary to fill the space between the adjacent gate electrodes with a resist pattern 111 having a width of $L3$. If the distance between the adjacent gate electrodes is shorter than $L2$, there is no need to form the resist pattern 111 between the adjacent gate electrodes.

(Other Embodiments)

This embodiment materializes a CAD software for producing a resist mask according to the rule explained referring to Figs. 35 to 40. This makes it possible to readily produce a reticle for forming the resist mask which can prevent the impurity introduced along a direction tilt-angled from getting into the source-and-drain region. This can be realized by running a program stored in an RAM or ROM of a computer. Also such program and a computer-readable storage medium having recorded therein such program also fall within a scope of the present invention.

More specifically, the program is provided to a computer while being stored in a recording medium such as CD-ROM, or other various transmission media. The recording media, besides CD-ROM, capable of storing the program include flexible disk, hard disk, magnetic tape, magneto-optical disk and non-volatile memory card. On the other hand, the transmission media for the program include a communication medium (such as connected line such as using optical fiber, or radio line) in a computer network system (e.g., LAN, WAN such as the Internet, radio communication network), whereby program information is transmitted as being modulated by a carrier wave.

The aforementioned program fall within a scope of the present invention not only for the case where the functions of the above-described embodiments are materialized by the supplied program run on a computer, but also for the case where the functions of the above-described embodiments are realized by the program in cooperation with an OS (operating system) run on the computer or with any other application software, and for the case where the functions of the above-described embodiments are realized by the whole or a part of the program executed on a function expansion board or function expansion unit of the computer.

For example, Fig. 41 shows a block diagram of an internal constitution of a general personal user

terminal device. In Fig. 41, reference numeral 1200 denotes computer PC. The PC 1200 has a CPU 1201, which is designed to execute a device control software stored in a ROM 1202 or a hard disk (HD) 1211, or supplied from a flexible disk drive (FD) 1212, so as to totally control the individual devices connected to a system bus.